Terahertz technology for ultra-broadband and ultra-wideband operation of
backhaul and fronthaul links in systems with SDN management of network and radio resources

TERAWAY

# Scalable Highly-Integrated Packaging for the 5G World: From Datacenters to Drones

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phix PHOTONIC ASSEMBLY

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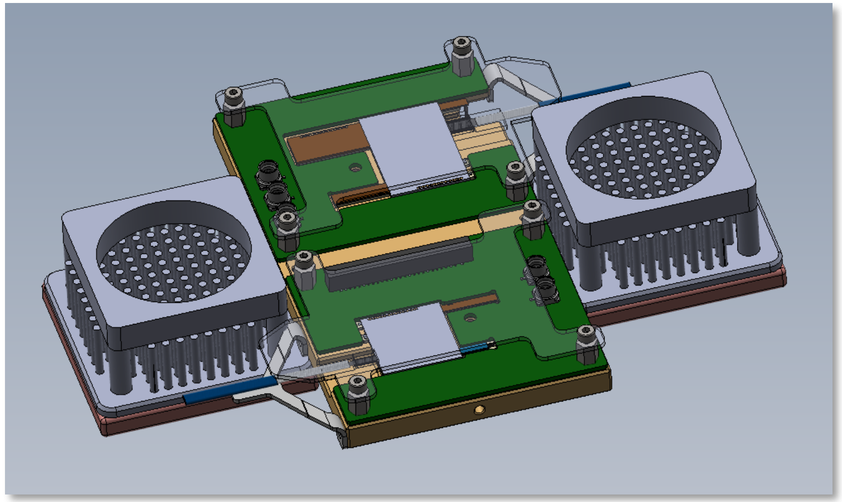
# Content

- Integration Trends for Photonics
- Introduction to TERAWAY
- Thermal Configurations for Highly-Integrated Systems
- Active Cooling Design with Peltier TECs
- Antenna Rod Placement



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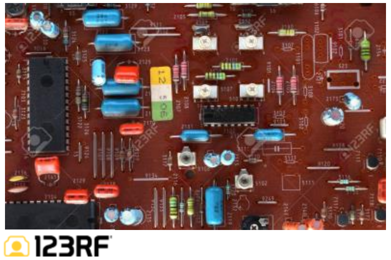
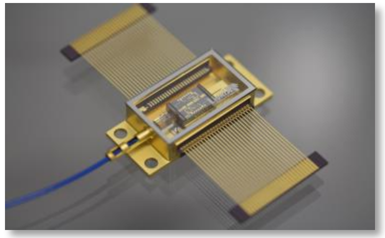
# Integration Trends

Devices → Systems

Individually-packaged devices

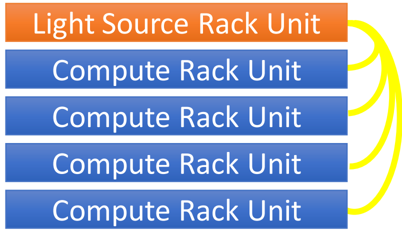



Every component (resistor, transistor, laser, PD, splitter, modulator) in its own package and connected with discrete fibers, wires, flex or PCB traces.

Circuit/system is built out of discrete components.

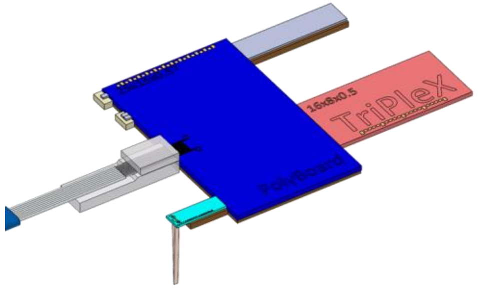
Integrated circuit in package with "hard parts" outside




Components that can be monolithically integrated (resistors, transistors, splitter, modulators) are in one package or even one die.

Components with special requirements are kept separate ("Light as a utility" laser, extremely-cold photodetectors)

Everything in the package





Hybrid (Luxtera, Mellanox), Heterogenous (Intel) integration of light source

Monolithic single-photon detector (PsiQ)

Hybrid integration of many disparate components (TERAWAY/POETICS)

# Terahertz technology for ultra-broadband and ultra-wideband operation of backhaul and fronthaul links in systems with SDN management of network and radio resources

**Topic:** 5G Long Term Evolution

**Type:** RIA

**Call:** H2020-ICT-2019-2

**Contract No:** 871668

**Start date:** 1 November 2019

**Duration:** 36 Months

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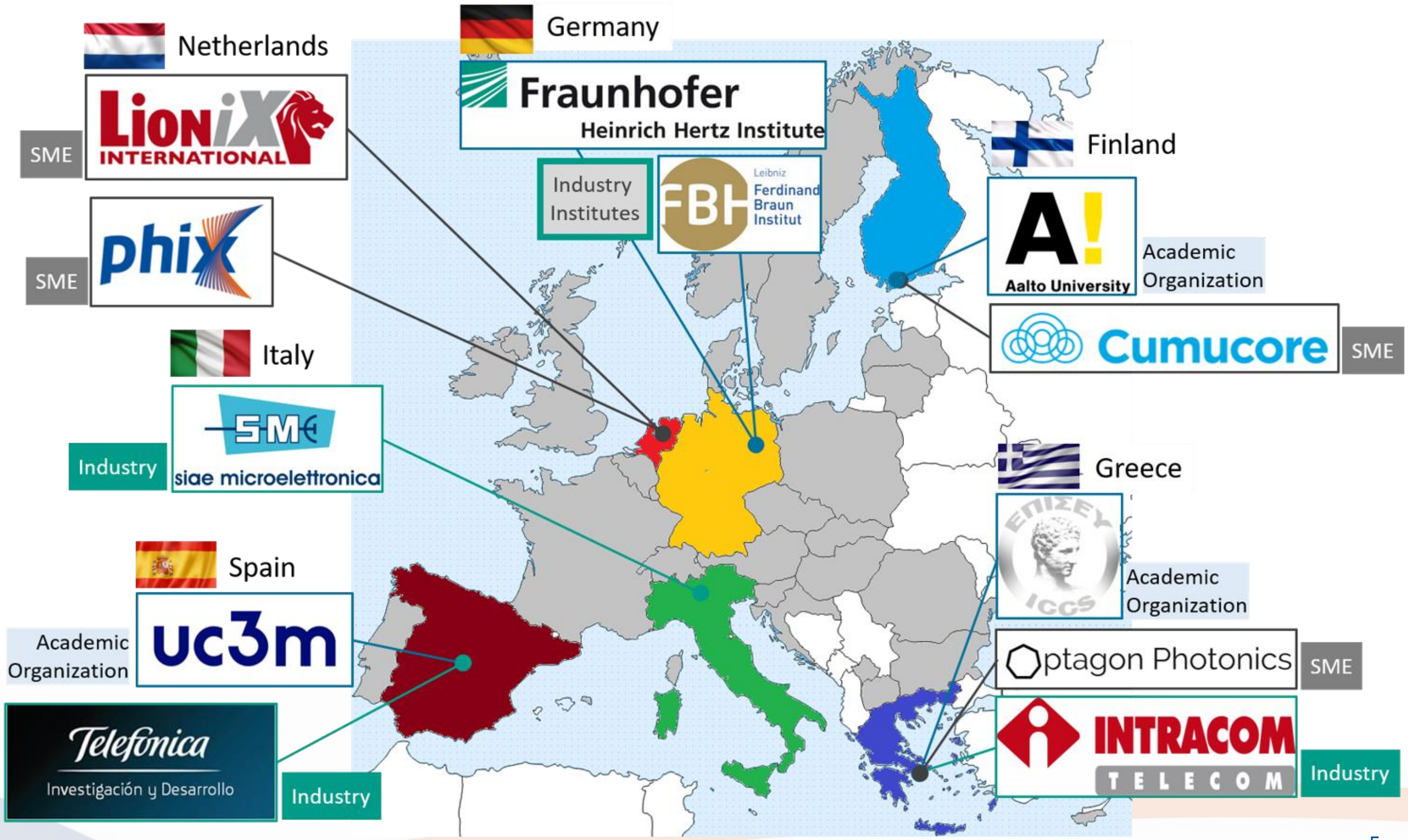
# TERAWAY Consortium

## 12 Partners
## 6 EU countries

- **3** Large Companies
- **4** SMEs
- **2** Industry-oriented Research Institutes
- **3** Academic Organizations



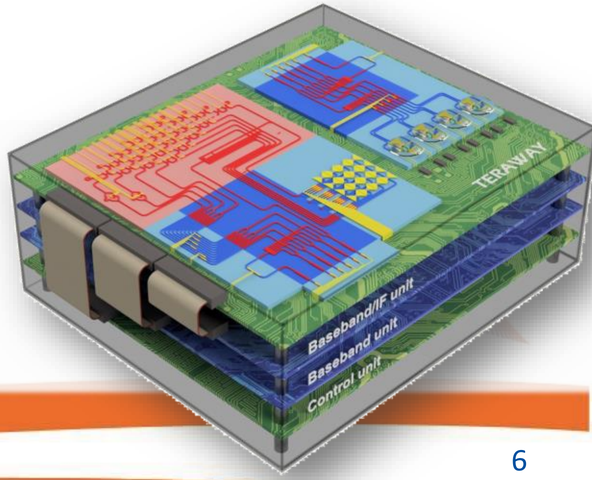
# TERAWAY Project

## A new disruptive generation of photonic-enabled THz transceivers for high-capacity BH and FH links in 5G networks.

## Vision- Concept

*"enabling industrialization of THz wireless communication technology"*

- **Development of a common technology base for the generation, emission and detection of wireless signals in the THz (252–322 GHz) and W/D bands**
- **Multi-channel, ultra-wide band transmitters**: Generation/emission of THz/W/D signals with selectable symbol rate, high bandwidth and of high transmission reach
- **Multi-channel, ultra-wide band receivers**: Detection of THz/W/D band signals and their direct down-conversion to baseband
- **Integration of the nodes inside a functional network system of high-flexibility and efficiency:** New network management platforms (based on SDN) and an extended control hierarchy to perform the management of the network and radio resources.

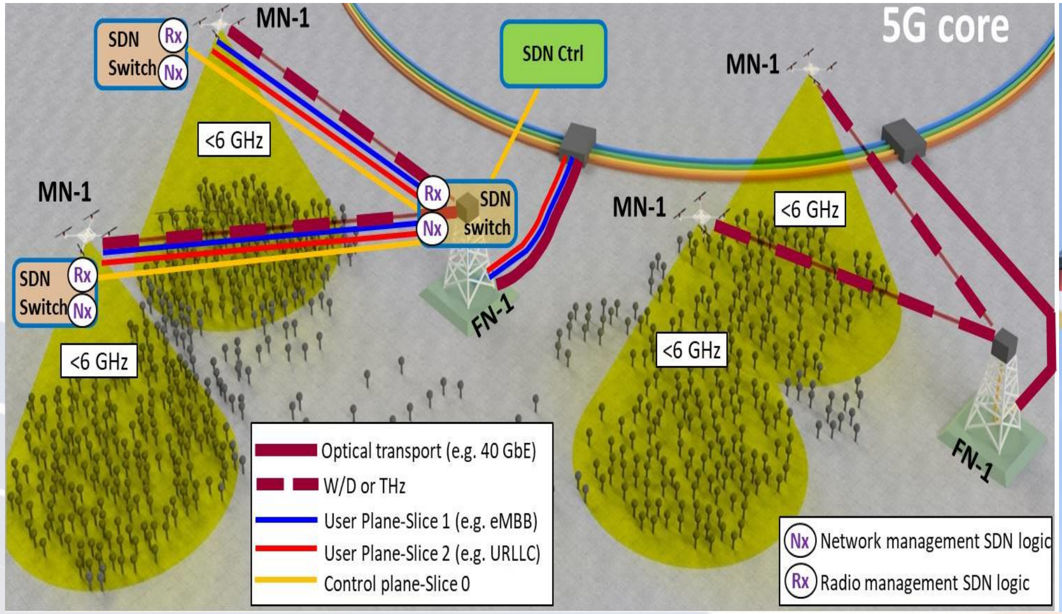


# TERAWAY Project

## A new disruptive generation of photonic-enabled THz transceivers for high-capacity BH and FH links in 5G networks.

## Application- Demo scenarios

Communication and surveillance coverage of outdoor mega-events using fixed and moving nodes in the form of heavy-duty drones, carrying either gNBs or solely their radio parts.




**TERAWAY Technology**
Enabling new applications of commercial and societal interest

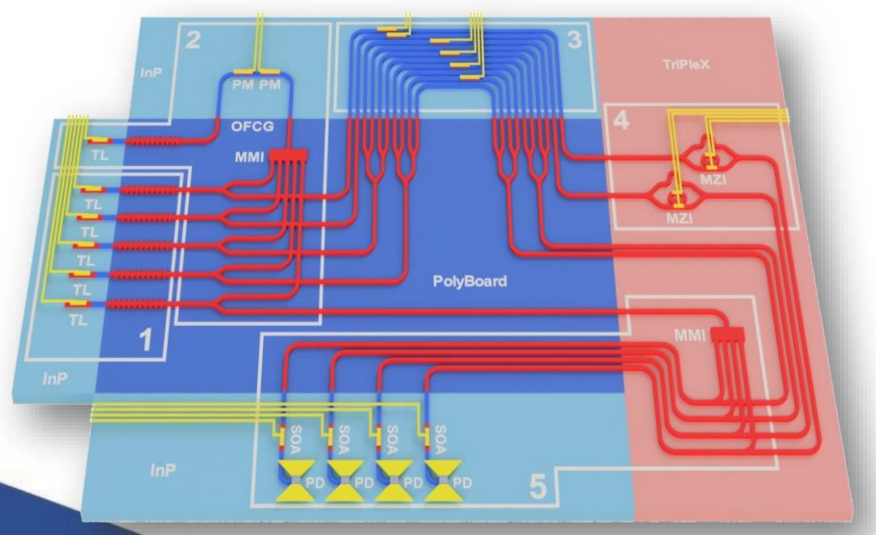
# TERAWAY high-capacity W/D/THz transceivers

## **Hybrid photonics-based platform** for ultra-wideband signal generation and emission

Objective 1

Objective 2

Transmitter




**1. Optical carrier generation unit**
Tunable Lasers (TLs): Free selection of the emission wavelength over a range of more than 10 nm

**2. Optical phase locking unit**
Optical Frequency comb generator (OFCG) + optical circuit: low phase noise

**3. Optical modulation unit**
Phase Modulators for • low-capacity links (2.16 GHz bandwidth) and • IQ Modulators for high-capacity links  (25.92 GHz)

**4. Optical filtering unit**

**5. Optical multi-beamforming unit**
Independent steering of the transmitted wireless beam

**6. Optical amplification, frequency up- conversion and wireless emission unit**
Use of semiconductor optical amplifiers, PIN-  photodiodes as photonic mixer and bow-ties antennas

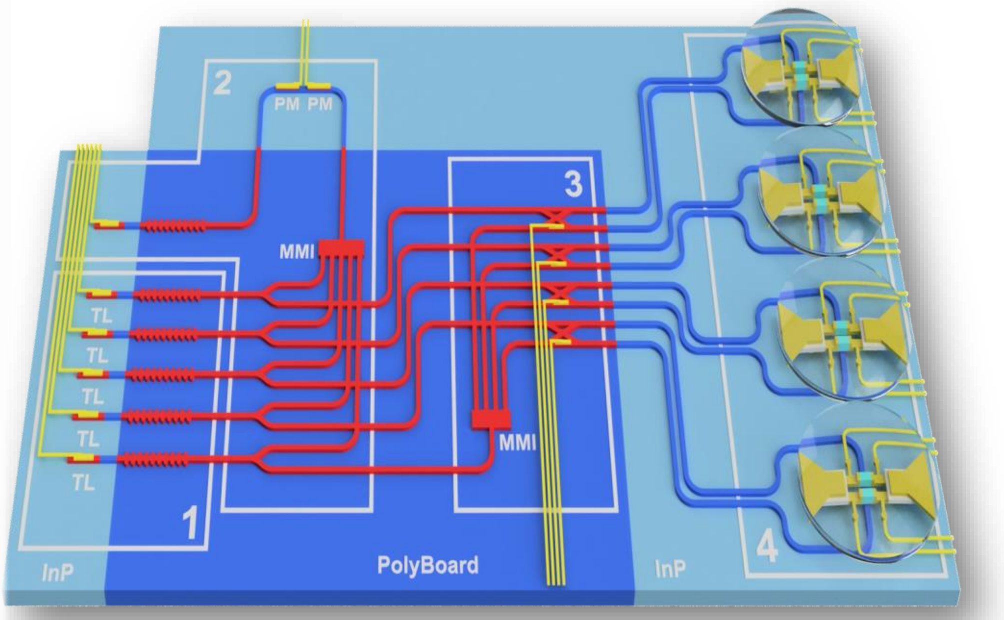
# TERAWAY high-capacity W/D/THz transceivers

## **Hybrid photonics-based platform** for ultra-wideband signal detection and reception

### Objective 3

1. **Optical carrier generation unit**
   Same as transmitter
2. **Optical frequency comb generator unit**
   Same as transmitter
3. **Optical phase shift unit**
   Introduction of 90° phase difference between copies of the same optical carrier
4. **Wireless detection and IQ photonic mixing unit**
   Use of bow-tie antennas with silicon lenses and photoconductive elements for down-conversion to the baseband
   Development of low-noise and high bandwidth TIAs

Receiver



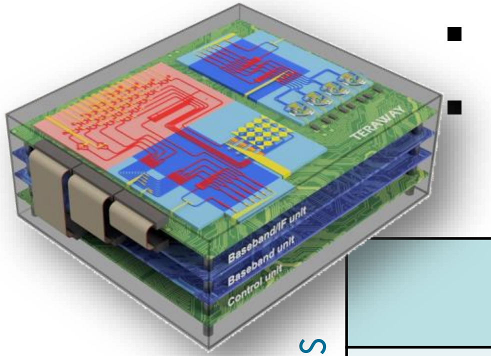
# TERAWAY Modules

## **Multi-channel transceiver Modules** with total capacity up to 241 Gb/s

**Objective 4**

Development and integration of 4 Transceiver Modules

- Modules -1, -2 (Precursor units)
- Modules -3, -4 (Main Transceiver Modules)




System specifications

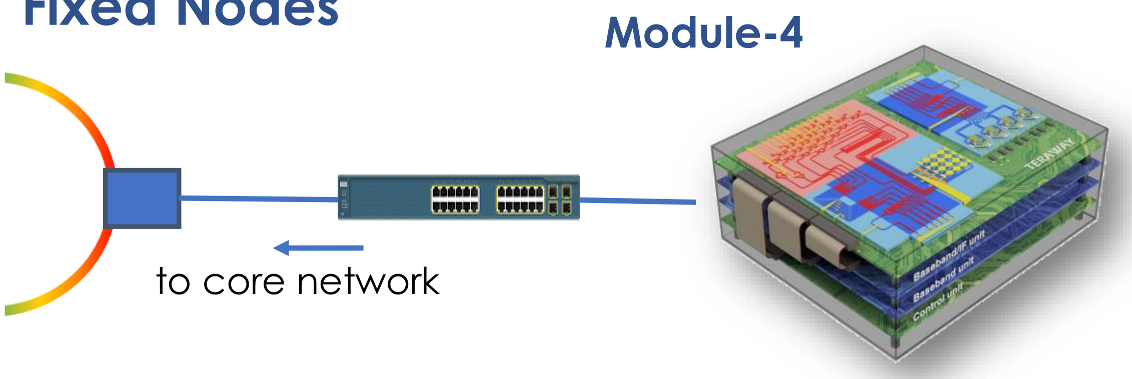
| TERAWAY Module | Tx Module-1 (Precursor) | Tx Module-2 (Precursor) | Tx Module-3 (Main Module) | Tx Module-4 (Main Module) |
|---|---|---|---|---|
| # of channels | 1 | 1 | 2 | 4 |
| IF or baseband | IF | Baseband | 1 IF / 1 Baseband | 2 IF / 2 Baseband |
| Symbol rate (Gbaud) | ~1.5 | 18 | 1.5 / 18 | 2x1.5 / 2x18 |
| Modulation format | Up to 256-QAM | Up to 64-QAM | 256-QAM / 64-QAM | 256-QAM / 64-QAM |
| Total bit rate (Gb/s) | ~ 12.5 | 108 | 120.5 | 2x120.5 |
| OBFN | NO | 1x4 Blass matrix | 2x16 Blass matrix | 4x16 Blass matrix |
| Electrical units | Modem, CU | | | |
| Operation band | W/ D/ THz | | | |

# TERAWAY Systems Engineering

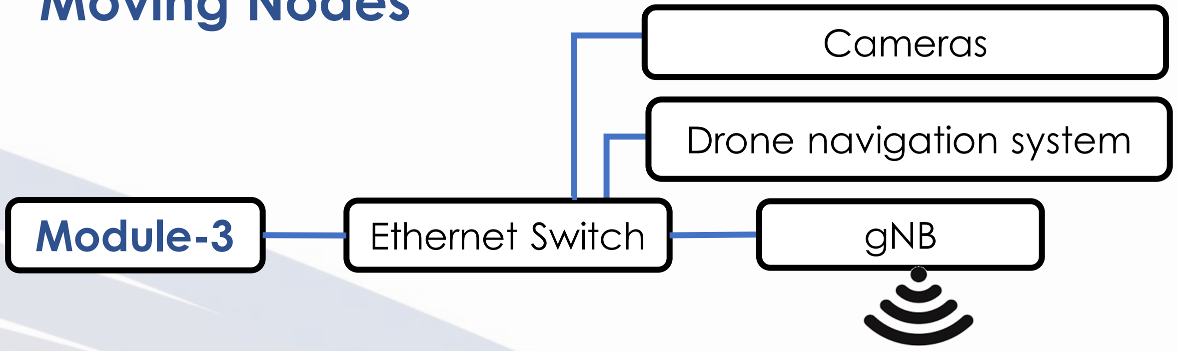
## **Network Nodes** for BH and FH connectivity

### Objective 5

### Fixed Nodes




### Moving Nodes




## **THz propagation** model & localization techniques

### Objective 6

Development of 3D path-loss map

Development of localization algorithms

## **Network management** and application tools

### Objective 7

Optimum use of network and radio resources and accommodation of eMBB and URLLC services

- SDN platform
- Slicing manager
- Platform for processing of surveillance data

# Work plan - Roles of partners

## Modules development, DSP toolbox

- Development of the transceivers
- Integration and packaging of the transceivers
- Integration and packaging of the Modules
- Development of DSP tools and algorithms
- Testing of Modules in lab

## Network management, Nodes development, System experiments & Field trials

- Network management & slicing techniques
- Development of SDN agents
- THz propagation models, localization techniques, link establishment
- Integration and packaging of the Nodes
- Testing of Nodes in campus
- System Field trials

# Work plan - Roles of partners

## Modules development, DSP toolbox

- Development of the transceivers
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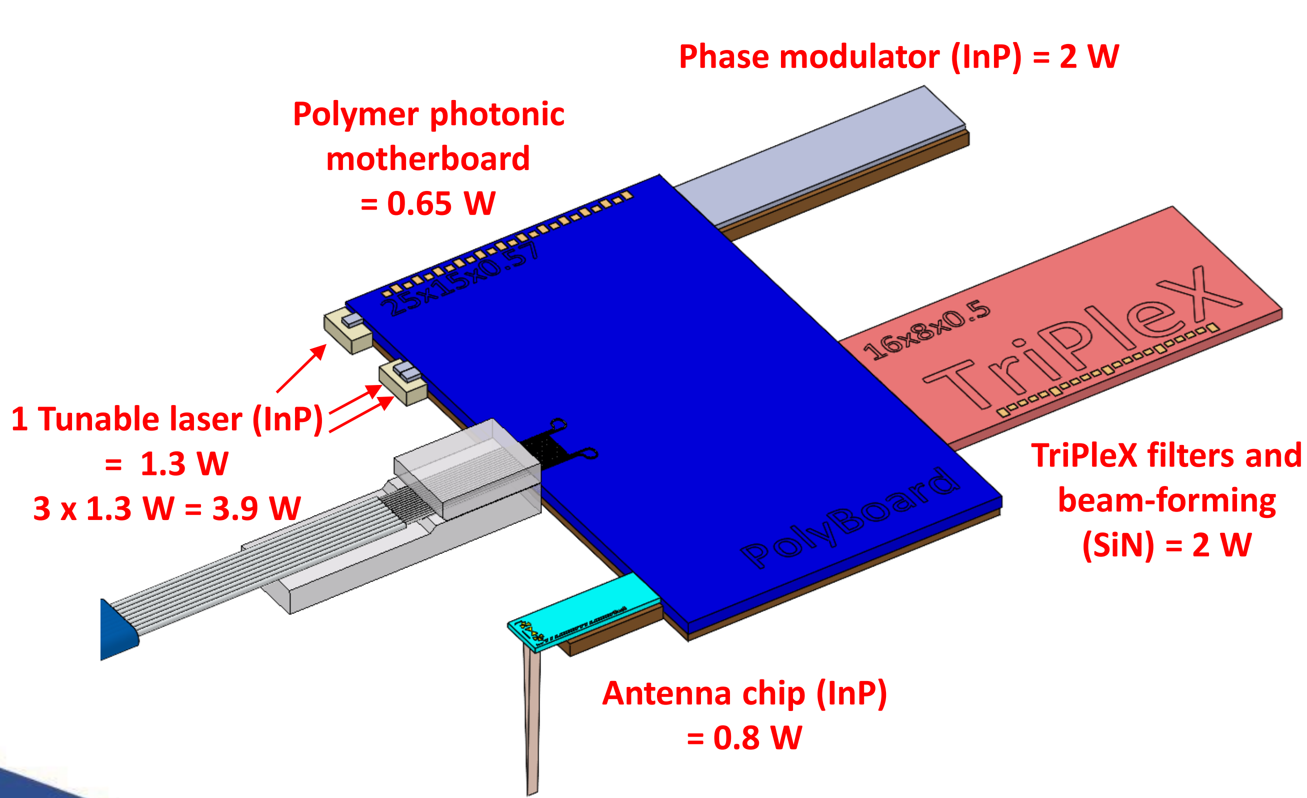
Fraunhofer Heinrich Hertz Institute
LioniX International
uc3m
ICCS
Optagon Photonics
INTRACOM TELECOM
FBH Leibniz Ferdinand Braun Institut

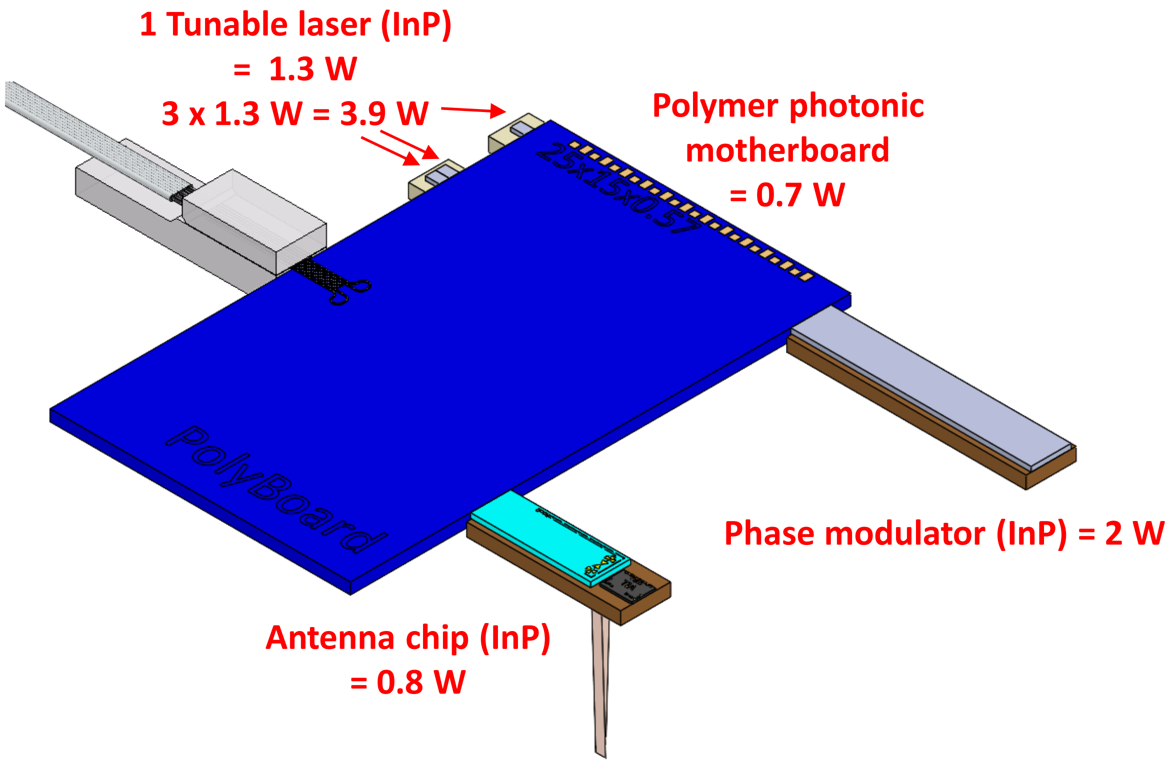
phix

# TERAWAY Module 1 Physical Model

## Transmitter




## Receiver




- PHIX design rules require the optical and electrical interfaces to be on different edges
- Multiple optical interfaces/components can coexist on a single edge if spacing requirements are respected

# TERAWAY Module 1 Thermal Breakdown

| Transmitter components | Max. Power Consumption (W) | Max. Heat Dissipation (W) | Operating Temperature (°C) | Maximum Temperature* (°C) |
|---|---|---|---|---|
| Tunable lasers (InP, 3x) | 6.9 | 3.9 | 25 | 100 |
| Phase modulator (InP) (incl. driver) | 2.0 | 2.0 | 20-50 | 260 |
| TriPleX (SiN) | 2.0 | 2.0 | 25-60 | 150 |
| Antenna chip (InP) | 1.0 | 0.8 | 25 | 100 |
| Photonic motherboard (PolyBoard) | 0.65 | 0.65 | 25 | 100 |

| Receiver components | Max. Power Consumption (W) | Max. Heat Dissipation (W) | Operating Temperature (°C) | Maximum Temperature* (°C) |
|---|---|---|---|---|
| Tunable lasers (InP, 3x) | 6.9 | 3.9 | 25 | 100 |
| Phase modulator (InP) | 2.0 | 2.0 | 20-50 | 260 |
| Antenna chip (InP) (incl. TIA) | 1.0 | 0.8 | 25 | 100 |
| Photonic motherboard (PolyBoard) | 0.7 | 0.7 | 25 | 100 |

**Heat Dissipation**

Tx = 9.35 W

Rx = 7.4 W

Total = **16.75 W**

**Operating Range**

**20-25 °C**

* For curing and solder reflow in later assembly steps

# TERAWAY Module 1 Thermal Breakdown

| Transmitter components | Max. Power Consumption (W) | Max. Heat Dissipation (W) | Operating Temperature (°C) | Maximum Temperature* (°C) |
|---|---|---|---|---|
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| Phase modulator (InP) (incl. driver) | 2.0 | 2.0 | 20-50 | [illegible] |
| TriPleX (SiN) | 2.0 | 2.0 | 25-60 | [illegible] |
| Antenna chip (InP) | 1.0 | 0.8 | 25 | [illegible] |
| Photonic motherboard (PolyBoard) | 0.65 | 0.65 | 25 | [illegible] |

| Receiver components | Max. Power Consumption (W) | Max. Heat Dissipation (W) | Operating Temperature (°C) | Te[illegible] (°C) |
|---|---|---|---|---|
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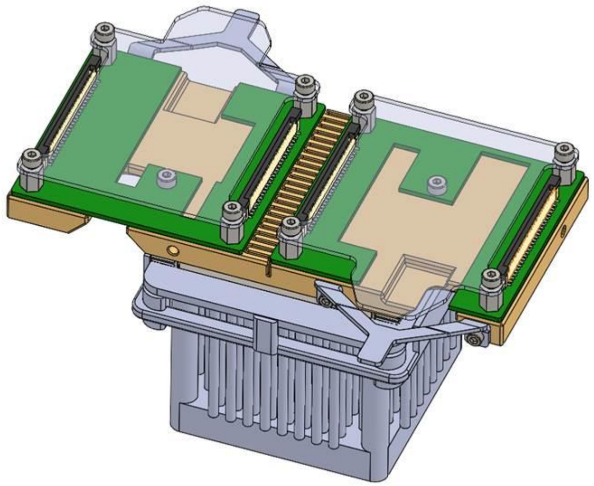
| Phase modulator (InP) | 2.0 | 2.0 | 20-50 | 260 |
| Antenna chip (InP) (incl. TIA) | 1.0 | 0.8 | 25 | 100 |
| Photonic motherboard (PolyBoard) | 0.7 | 0.7 | 25 | 100 |

In a less-integrated approach, the **sensitive components** could be partitioned from those that **generate a lot of heat** but are less sensitive. One challenge of TERAWAY is to bring them together in a fully-integrated system.

# Thermal Management Configurations

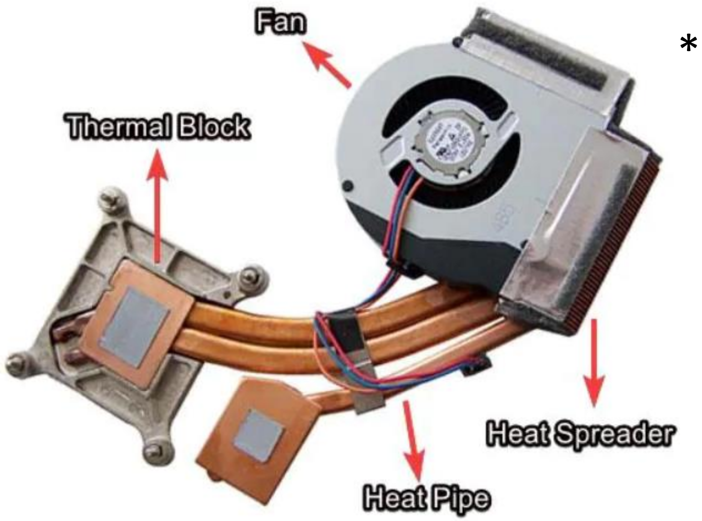
The default scenario is a TEC and heat sink mounted directly to the package submount of the module. However, …



Because of the presence of closed-loop monitoring and Peltier and/or forced convection, both of these are considered **active cooling** schemes.

- If the components could operate around 50 °C, we could avoid having a TEC altogether and use just one heat sink.
- Temperature could be regulated by controlling the fan speed, which would in turn change the thermal resistance of the fan.
- Thermal time constant of this modulation would need to be considered.

# Collective Heat Sinking with Heat Pipes

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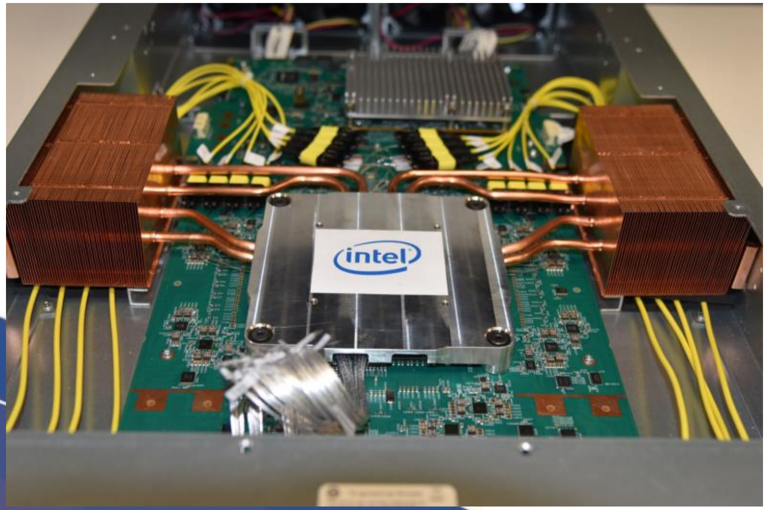
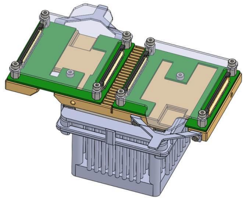


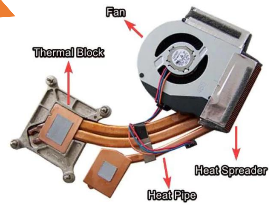

- It may make more sense to make a full system-level design for heat management rather than handling it module-by-module.
- Transceiver interface to the global heat management can be realized by (Cu) heat pipes.
- This enables larger heat sinks in more convenient locations and increased heat removal.

* Source: Any PC Part *via* https://www.msi.com/blog/laptops-101-understanding-what-goes-into-designing-an-efficient-laptop-cooling-solution

# Summary of options

Initial design was performed with first option, but elements of third were added in anticipation of final design.

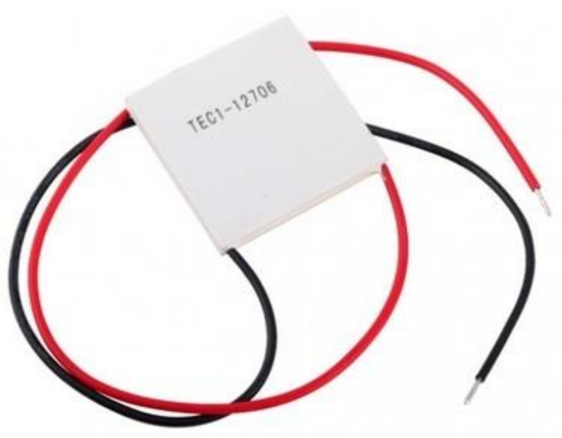





| | TEC + Heatsink directly on optical module | Heatsink only directly on optical module | TEC at optical module with heat pipe to system-wide heatsink |
|---|---|---|---|
| Operating Temperature | 20 – 25 °C | 50 °C | 20 – 25°C |
| Mechanical concerns | Bulky, may block beam steering, not scalable to later modules | Bulky, may block beam steering, not scalable to later modules | Minimal mechanical intrusion, scalable |
| Design complexity | Moderate | Simple | Requires full-project coordination |
| Cooling response time | Quick | Slow | Quick |
| Thermal isolation | High | High | Potential for aggressor effect |

This option was ruled out because it didn't meet temperature requirements.

# A few points on TECs
# (or why you don't have one in your refrigerator)




- TECs are made for high temperature differences and small loads
  - They are great for cooling and stabilizing tiny semiconductor lasers in dry $N_2$ hermetic packages
- TECs are inefficient
- TECs don't make heat disappear!
  - They just move it around and allow you to stabilize temperature in a closed loop
  - Heat sinks are required to get heat out of the system efficiently
- The heat sink is in many ways more important than the TEC

# The vicious cycle of TECs

We start here with a high heat load

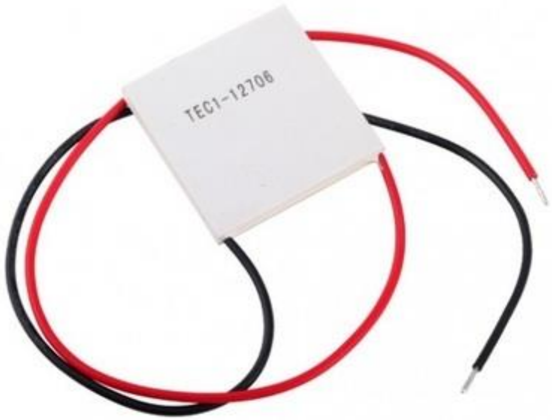
Heat load or temperature delta goes up

TEC becomes less efficient

TEC generates more waste heat

Heat sink has to dump more heat

Hot side temperature goes up



# Peltier Calculation

Whoa!!

Neither of these are exactly our case…
Graphs are hard to read…

**Calculate Starting Point**

Our heat dissipation =
**16.75 W (~ 5% $Q_{max}$)**

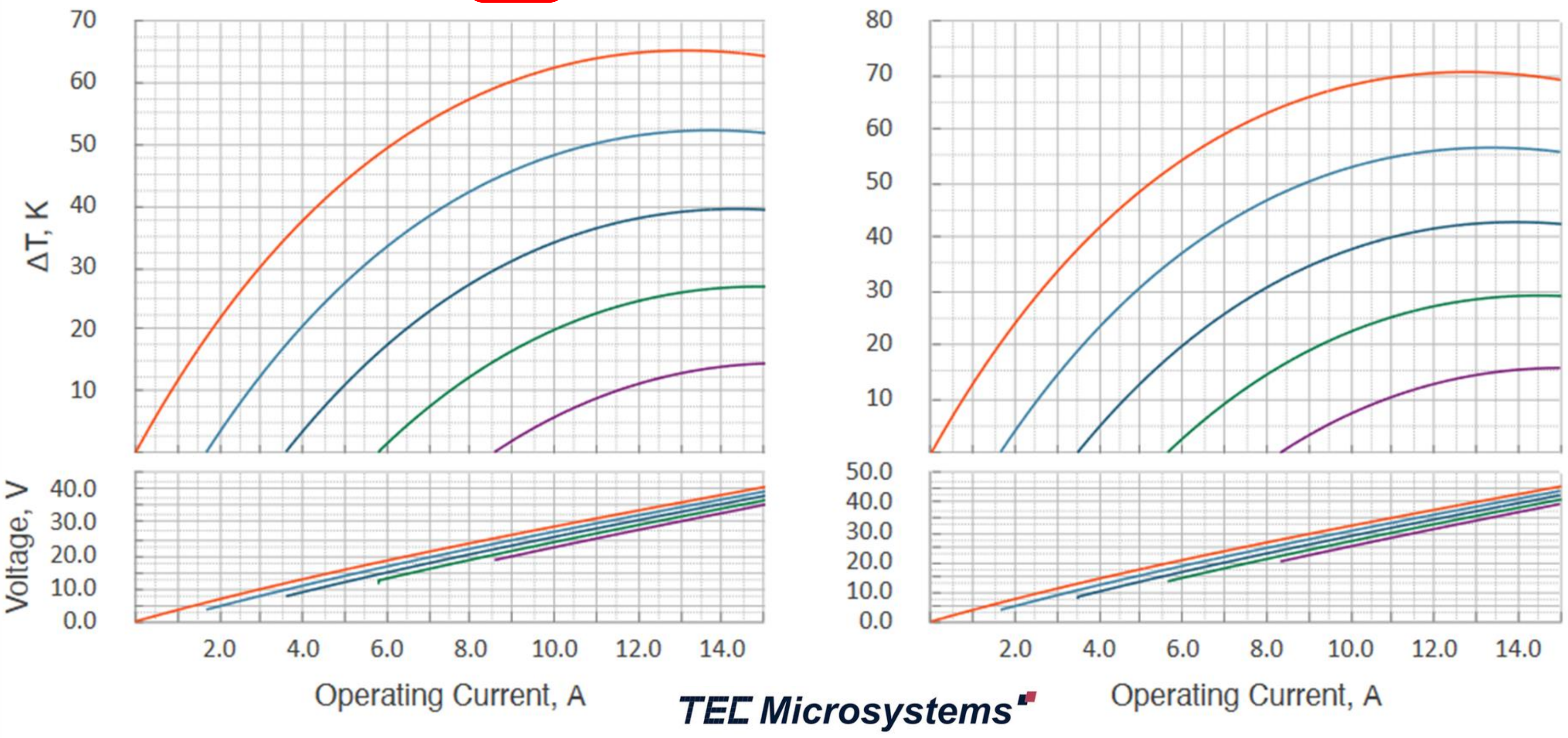
Hot side temperature ≥
300 K
+ 16.75 W*(0.51 K/W)
-> 35.39 °C

Operating Temp =
20.00 °C

ΔT =
**15.39 °C**

| @27°C, Vacuum | ΔTmax K | Qmax W | Imax A | Umax V |
|---|---|---|---|---|
| 1MA10-311-03 | 65 | 283.0 | 13.1 | 36.4 |

| @50°C, Dry N2 | ΔTmax K | Qmax W | Imax A | Umax V |
|---|---|---|---|---|
| 1MA10-311-03 | 71 | 304.6 | 12.8 | 39.6 |




| Heatload, W | 0.0 | 56.6 | 113.2 | 169.8 | 226.4 |
|---|---|---|---|---|---|
| % from Qmax | 0% | 20% | 40% | 60% | 80% |

| Heatload, W | 0.0 | 60.9 | 121.8 | 182.7 | 243.6 |
|---|---|---|---|---|---|
| % from Qmax | 0% | 20% | 40% | 60% | 80% |

# Peltier Calculation

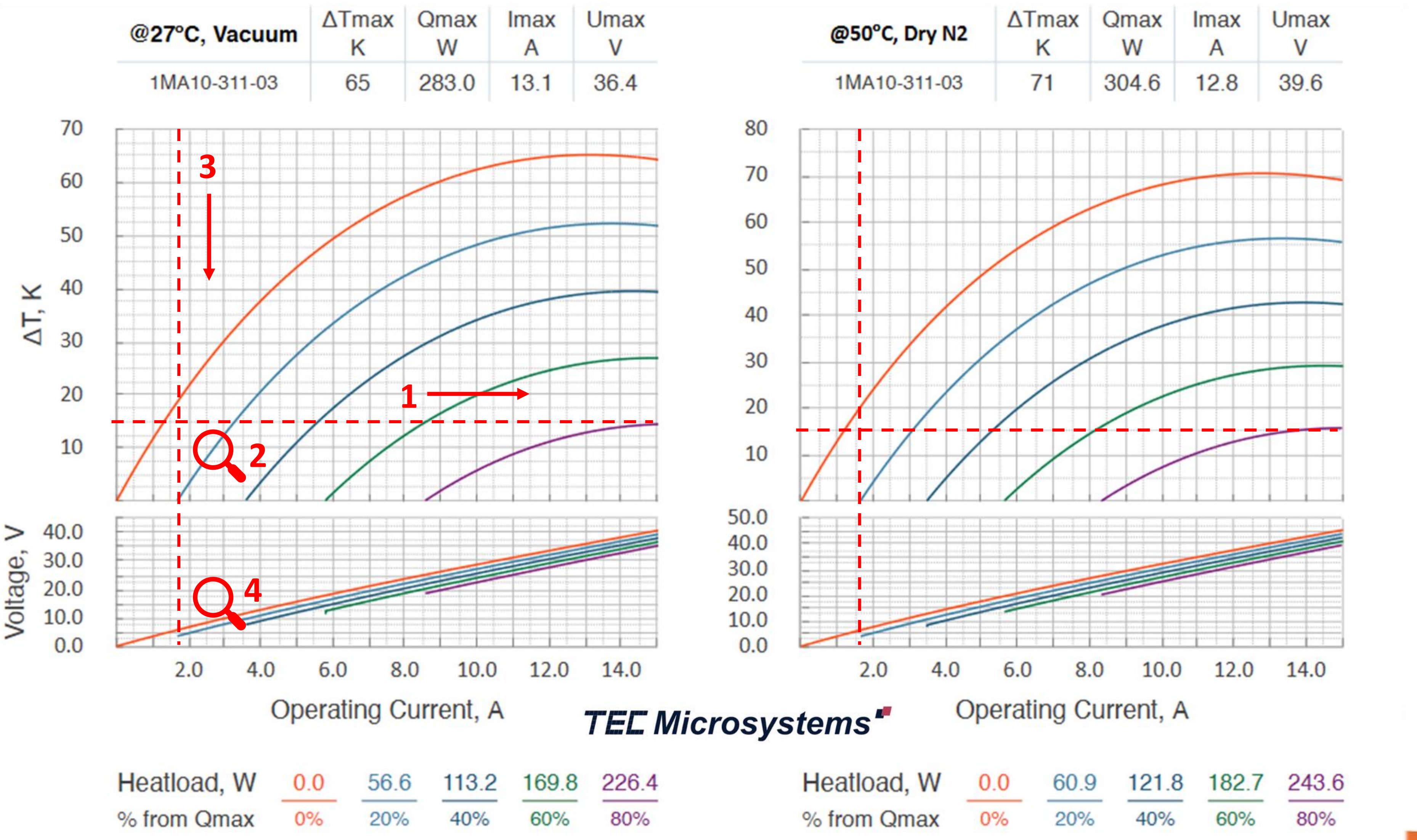
**Start Drawing Lines**

**$Q = \sim 5\% \ Q_{max}$**

**$\Delta T = 15.39\ °C$**

1) Draw horizontal line at ΔT
2) Walk horizontally along that line. 5% is about a quarter way between 0% and 20%.
3) Follow that line down to find the voltage and current operating points, again about quarter way between two plot lines.
4) Calculate waste heat:

   7(?) V * 1.7 A = **12 W**



# Peltier Calculation

Neither of these are exactly our case…
Graphs are hard to read…

**Re-Calculate Starting Point**

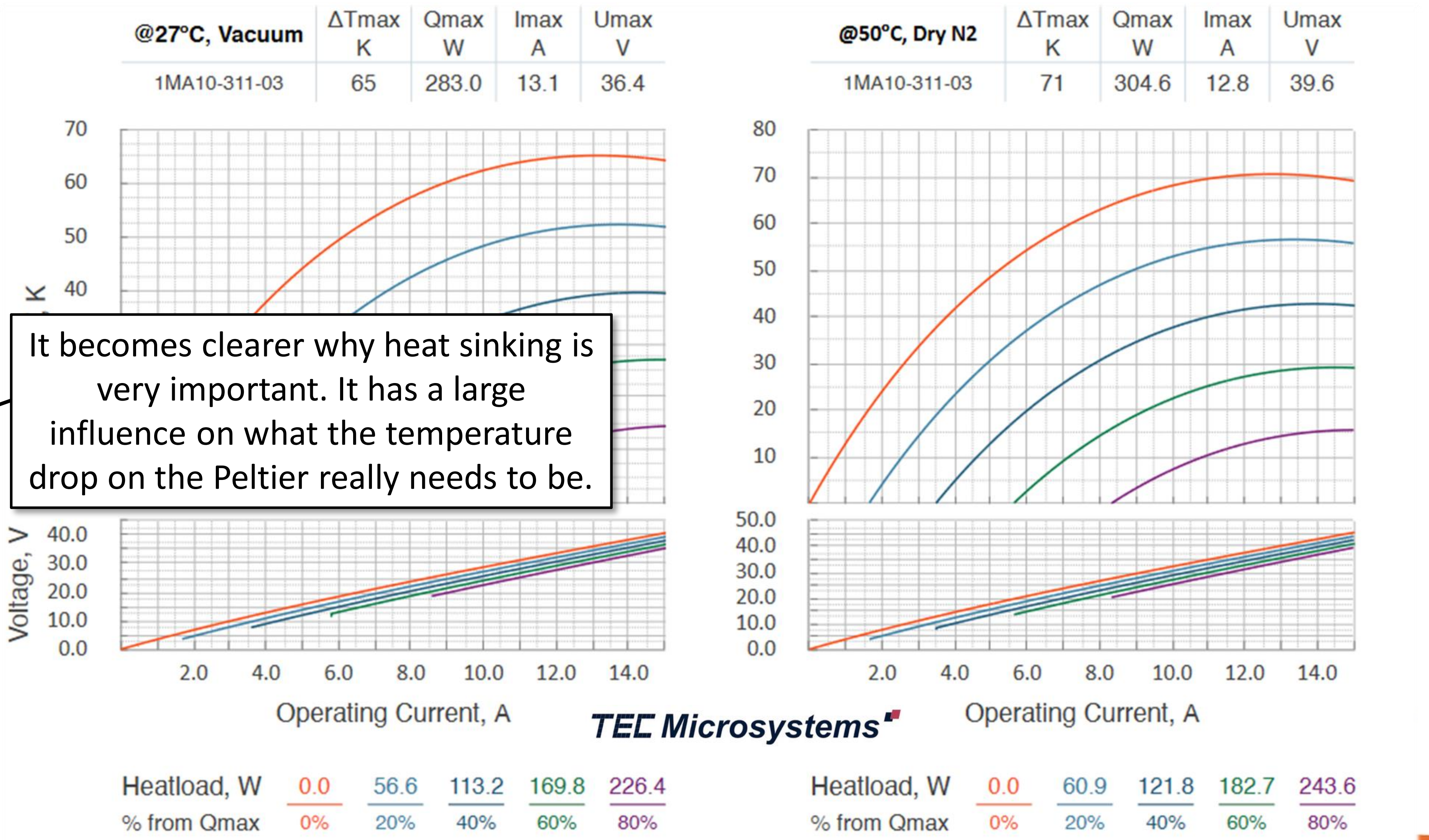
Our heat dissipation =
**16.75 W (~ 5% $Q_{max}$)**

Hot side temperature **now**
≥ 300 K
+ (16.75 W + 12 W)
*(**0.51 K/W**)
-> 41.7 °C

Operating Temp =
20.00 °C

ΔT **now** =
**21.7 °C**

It becomes clearer why heat sinking is very important. It has a large influence on what the temperature drop on the Peltier really needs to be.



# Peltier Calculation

**Drawing Lines Again**

**Q = ~ 5% $Q_{max}$**

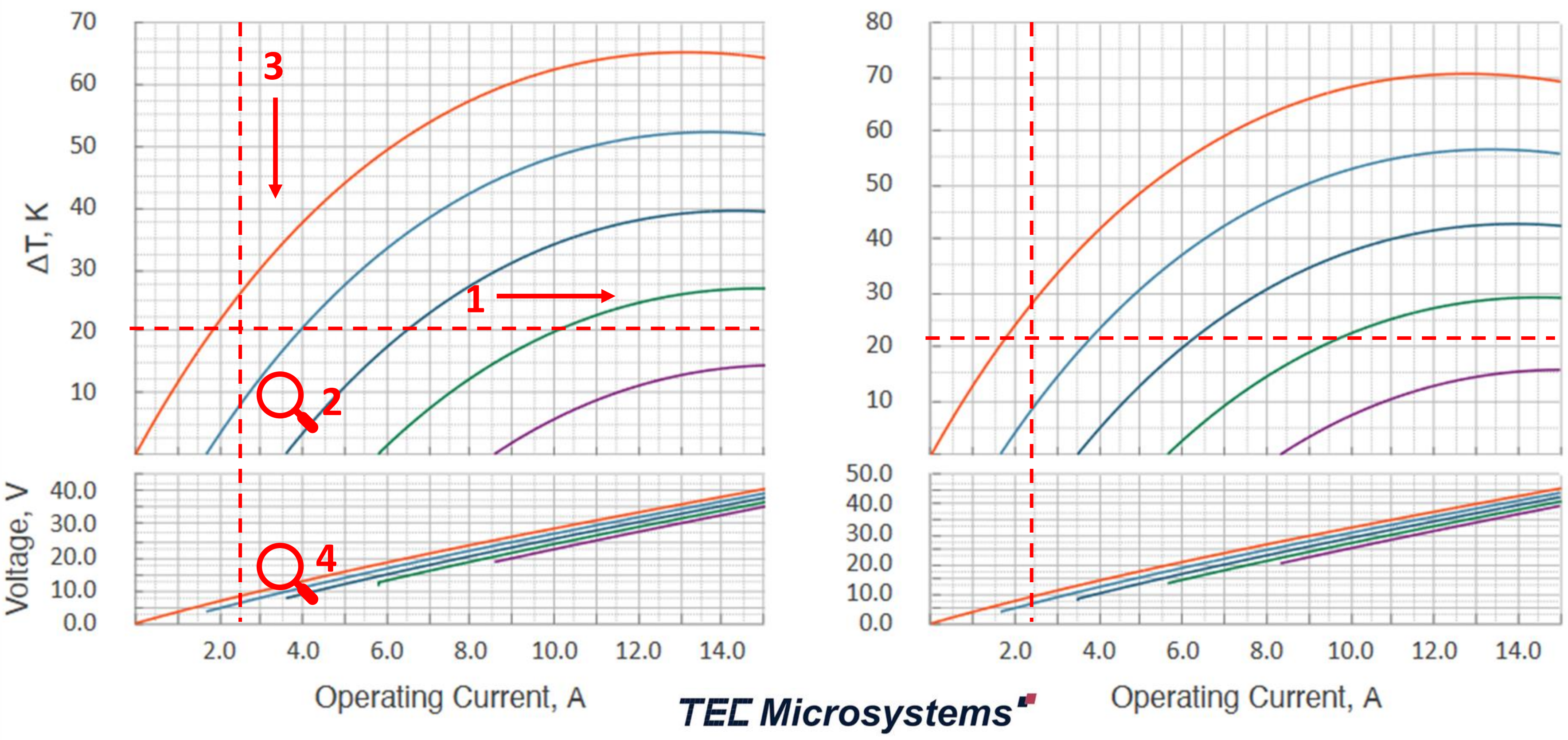
**ΔT = 21.7 °C**

1) Draw horizontal line at ΔT
2) Walk horizontally along that line. 5% is about a quarter way between 0% and 20%.
3) Follow that line down to find the voltage and current operating points, again about quarter way between two plot lines.
4) Calculate waste heat:

   9(?) V * 2.5 A = **22.5 W**

| @27°C, Vacuum | ΔTmax K | Qmax W | Imax A | Umax V |
|---|---|---|---|---|
| 1MA10-311-03 | 65 | 283.0 | 13.1 | 36.4 |

| @50°C, Dry N2 | ΔTmax K | Qmax W | Imax A | Umax V |
|---|---|---|---|---|
| 1MA10-311-03 | 71 | 304.6 | 12.8 | 39.6 |




| Heatload, W | 0.0 | 56.6 | 113.2 | 169.8 | 226.4 |
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| % from Qmax | 0% | 20% | 40% | 60% | 80% |

| Heatload, W | 0.0 | 60.9 | 121.8 | 182.7 | 243.6 |
|---|---|---|---|---|---|
| % from Qmax | 0% | 20% | 40% | 60% | 80% |

# Peltier Calculation

- Repeat the process until it converges…
- A Peltier with "perfect" heat sinking can have properties like this:

| Type | Parameters | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | ΔTmax [K] | Qmax [W] | Imax [A] | Umax [V] | τ [s] | R [Ohm] | Cold Size [mm²] | Hot Size [mm²] | Height [mm] |
| 2x1MC06-142-03 | 67 | 104.05 | 5.06 | 34.72 | 0.98 | 5.03 | 25.0x25.0 | 25.0x25.0 | 1.39 |

Thot = 300.0 [K], VACUUM

- But when an actual heat sinking situation is applied, the properties change to this:

| Type | Parameters | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | ΔTmax [K] | Qmax [W] | Imax [A] | Umax [V] | τ [s] | R [Ohm] | Cold Size [mm²] | Hot Size [mm²] | Height [mm] |
| 2x1MC06-142-03 | 32 | 28.16 | 2.14 | 18.51 | 0.95 | 5.03 | 25.0x25.0 | 25.0x25.0 | 1.39 |

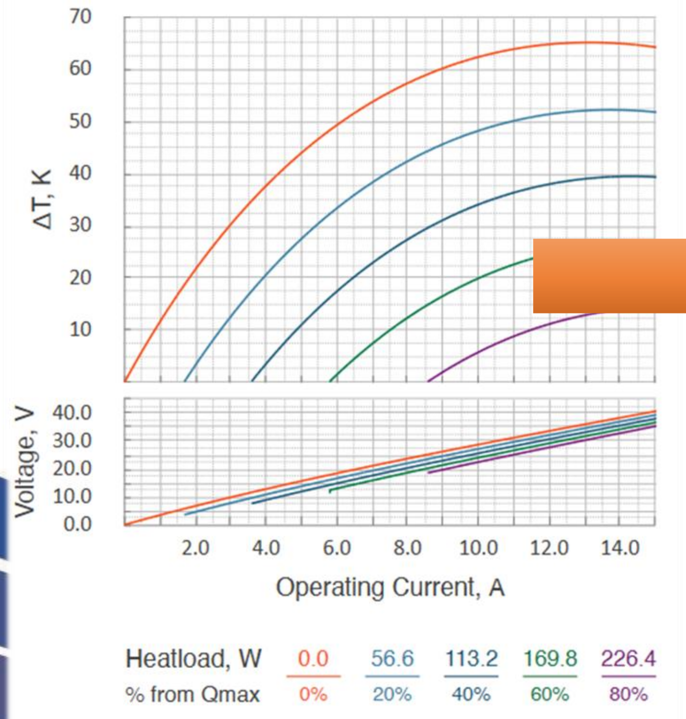
Thot = 300.0 [K], AIR, Heat Sink

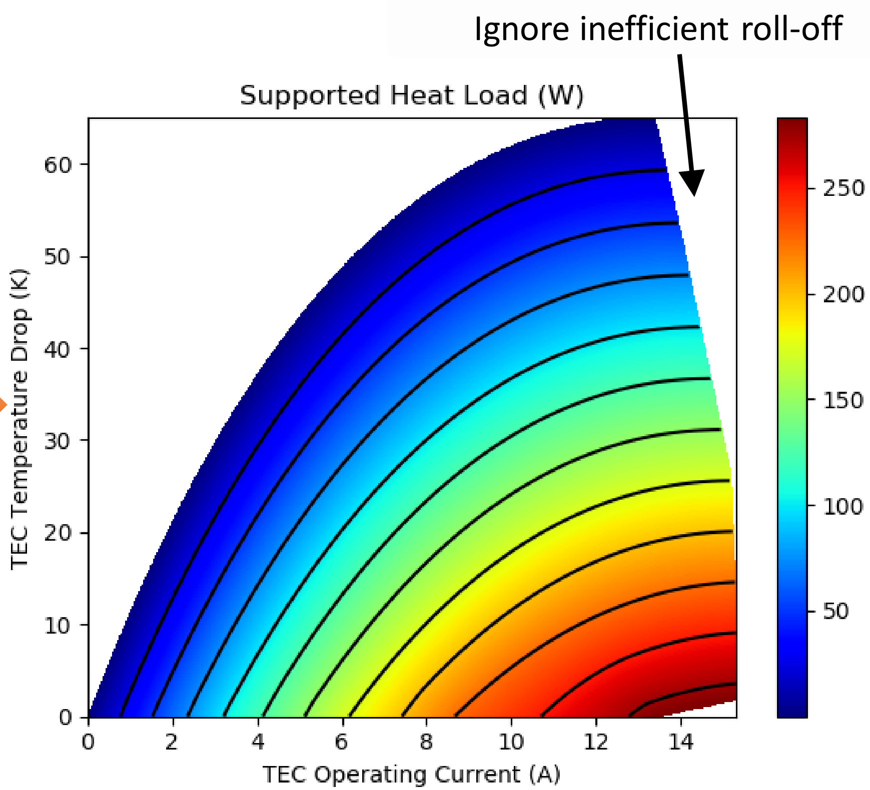
$Q_{max}$ went from **104 W** down to **28 W**(!)

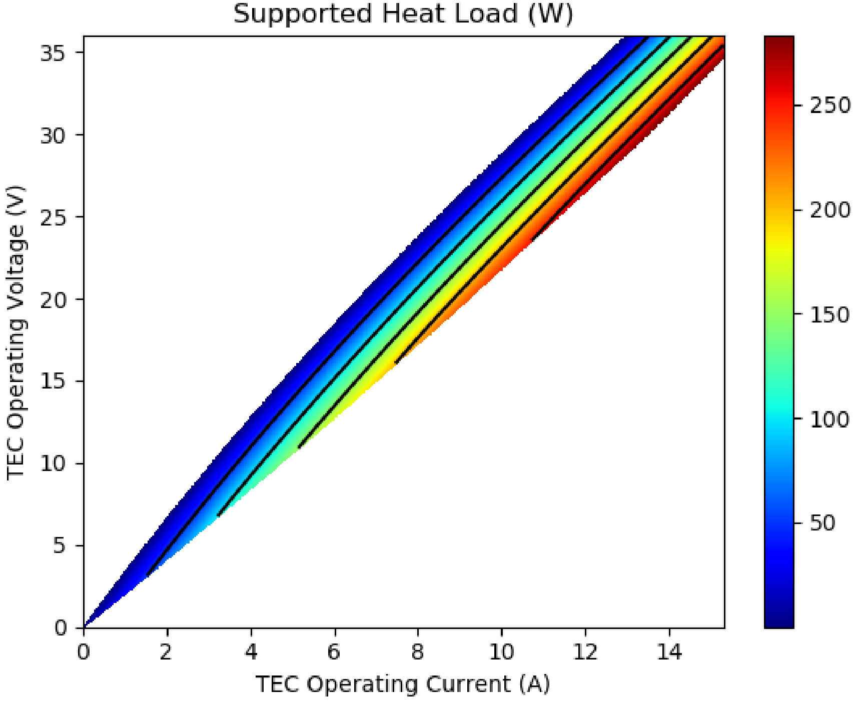
# Peltier Calculation (A Better Way)

- RMT Ltd. has a software called TECcad Lite that is good but only works for their TECs
- We wrote <u>in-house software</u> to scrape the data sheets of several vendors and interpolate them:

| @27°C, Vacuum | ΔTmax K | Qmax W | Imax A | Umax V |
|---|---|---|---|---|
| 1MA10-311-03 | 65 | 283.0 | 13.1 | 36.4 |

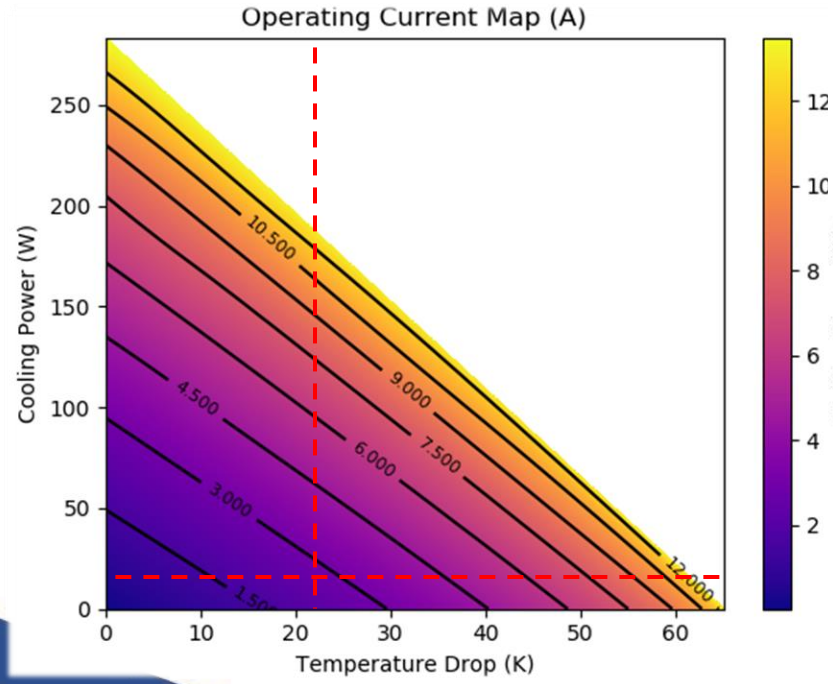


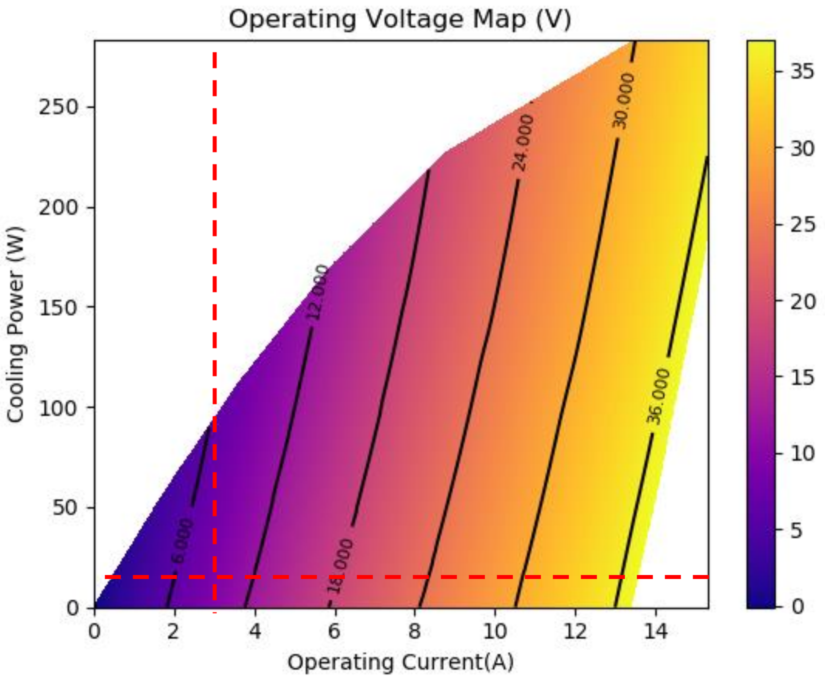



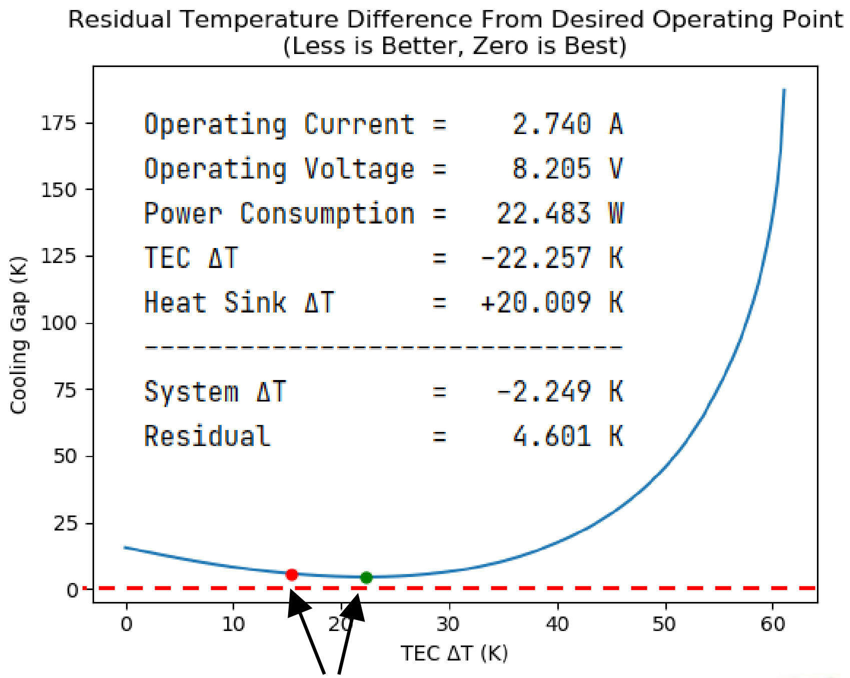



# Peltier Calculation (A Better Way)

- Our software builds operating point maps and does the iteration to find optimal solutions



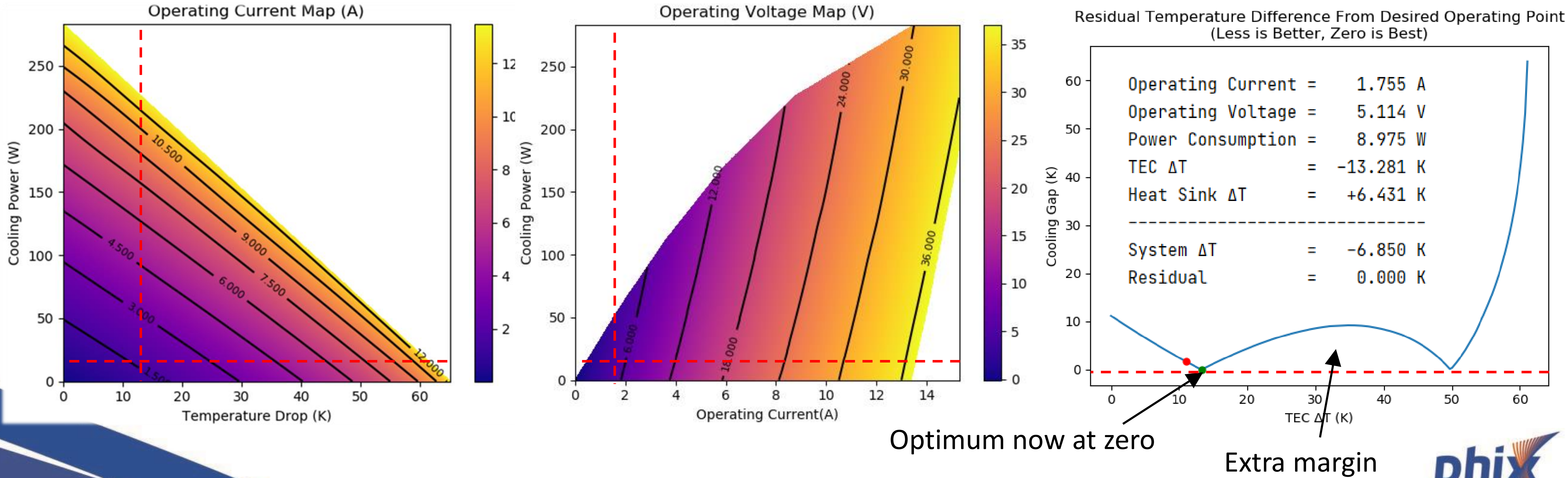




Starting guess (red)
Optimum (green)

In this case, the residual of **4.6 °C** means the heat sinking is not sufficient.

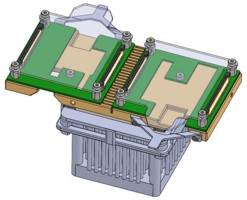
# Peltier Calculation (A Better Way)

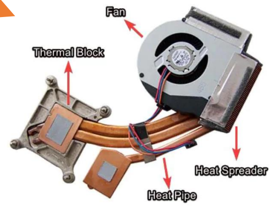
- In the previous example, if we improve the heat sink from **0.51 K/W** to **0.25 K/W**, the design now converges



# Summary of options (reminder)

Initial design was performed with first option, but elements of third were added in anticipation of final design.

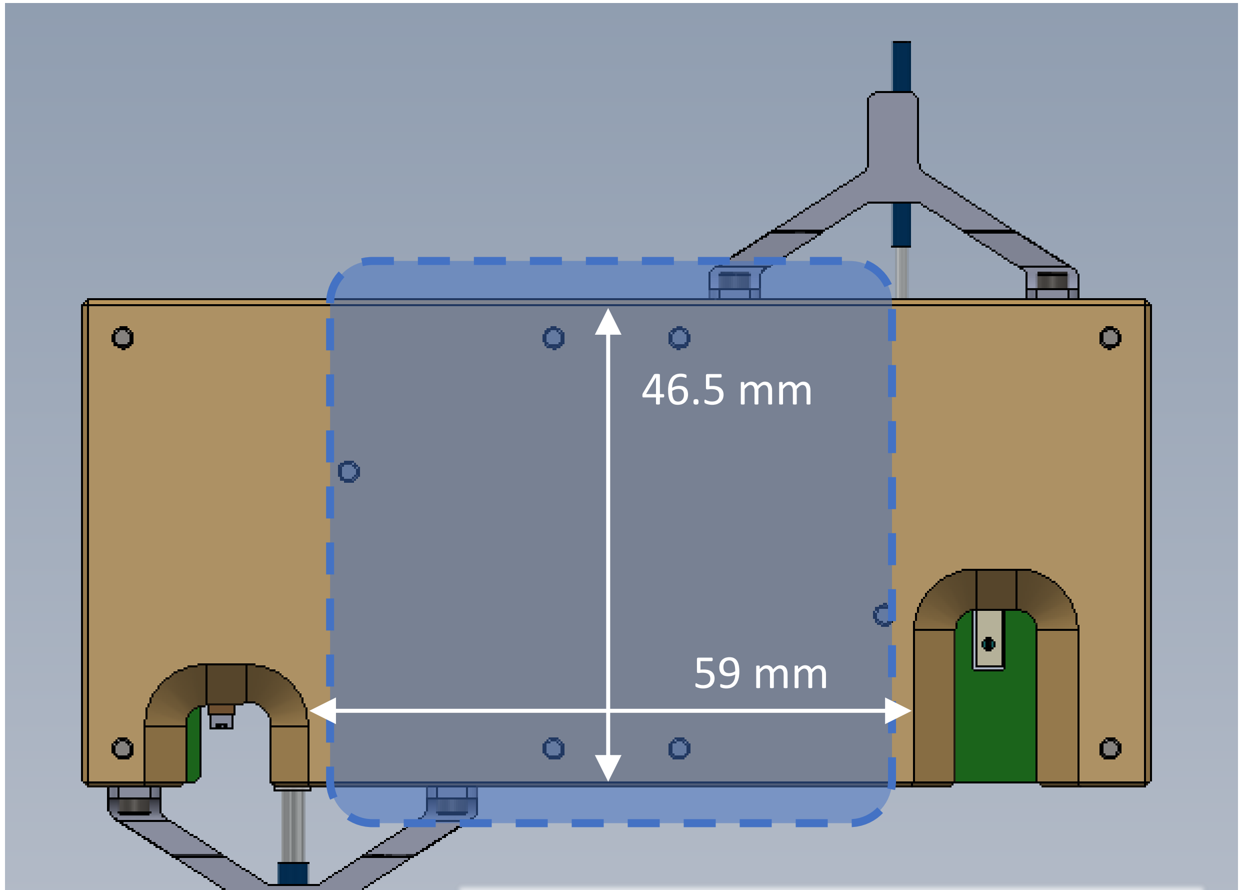





| | TEC + Heatsink directly on optical module | Heatsink only directly on optical module | TEC at optical module with heat pipe to system-wide heatsink |
|---|---|---|---|
| Operating Temperature | 20 – 25 °C | 50 °C | 20 – 25°C |
| Mechanical concerns | Bulky, may block beam steering, not scalable to later modules | Bulky, may block beam steering, not scalable to later modules | Minimal mechanical intrusion, scalable |
| Design complexity | Moderate | Simple | Requires full-project coordination |
| Cooling response time | Quick | Slow | Quick |
| Thermal isolation | High | High | Potential for aggressor effect |

This option was ruled out because it didn't meet temperature requirements.

# Thermal Management Sizing – Heat Sink

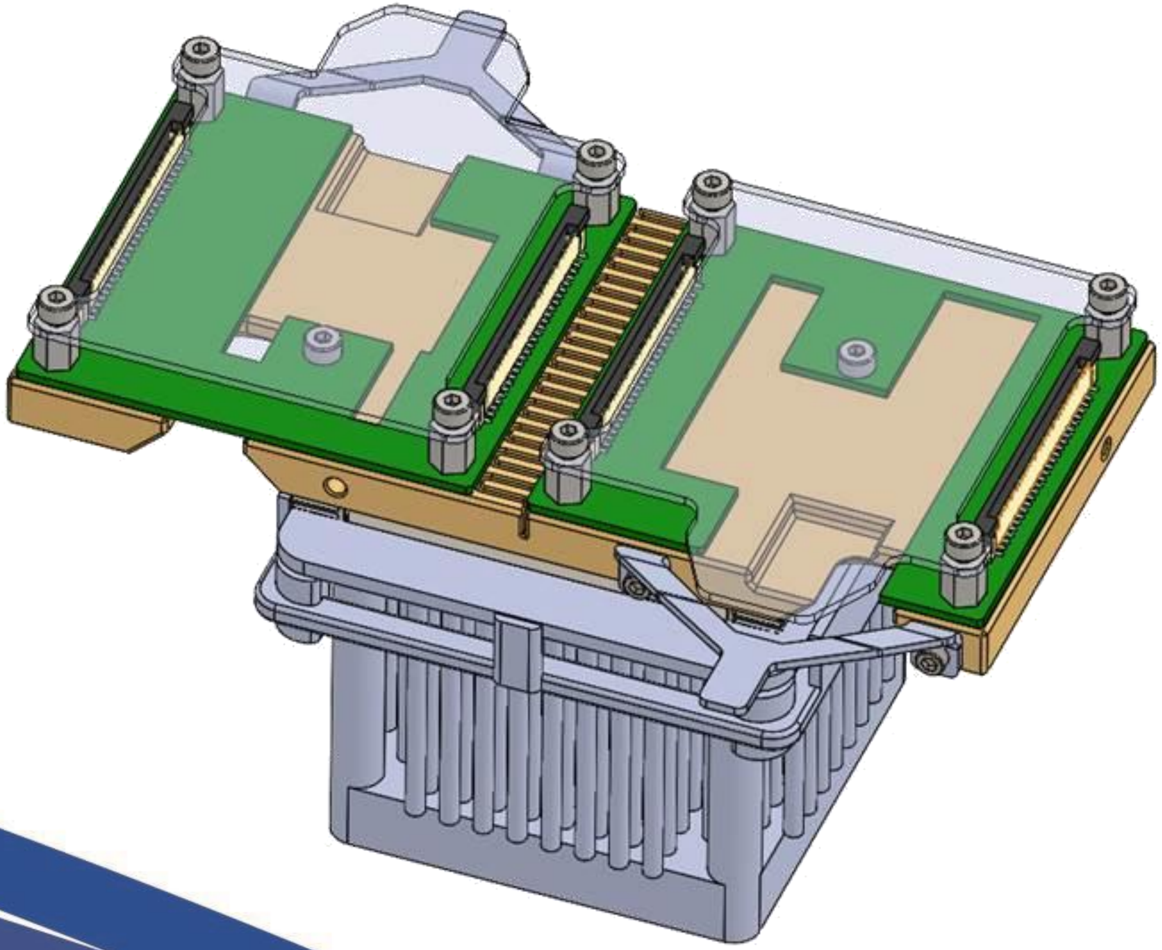



Cu submount sets limit of heat sink size. By overhanging slightly, we can get better performance.

| Part Number | Wakefield Solutions HSF-55-45-B-F |
|---|---|
| Footprint | 55 mm x 55.1 mm |
| Thermal resistance | 0.51 K/W |

For this small of footprint, this is the best we could find.

# Thermal Management Sizing – Heat Sink

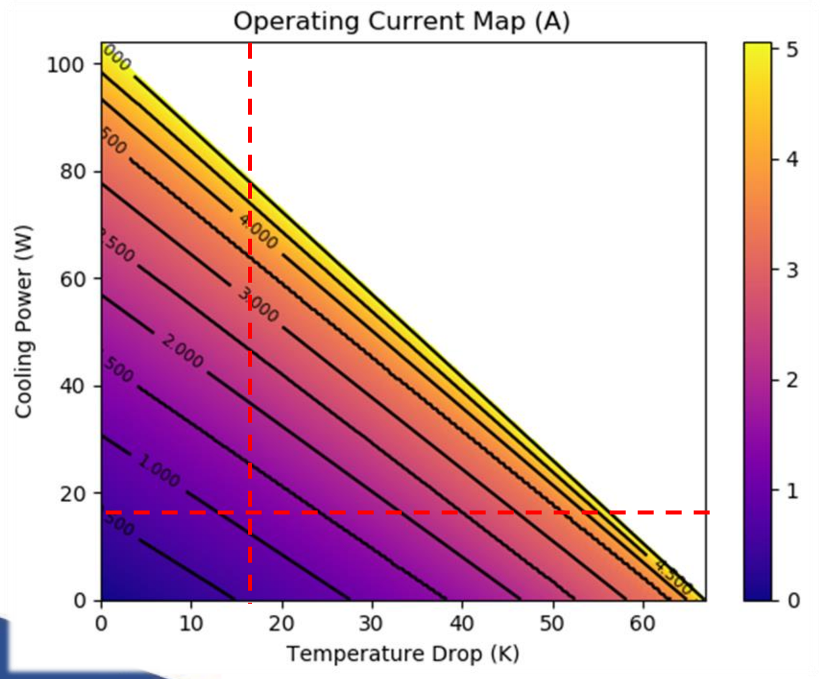


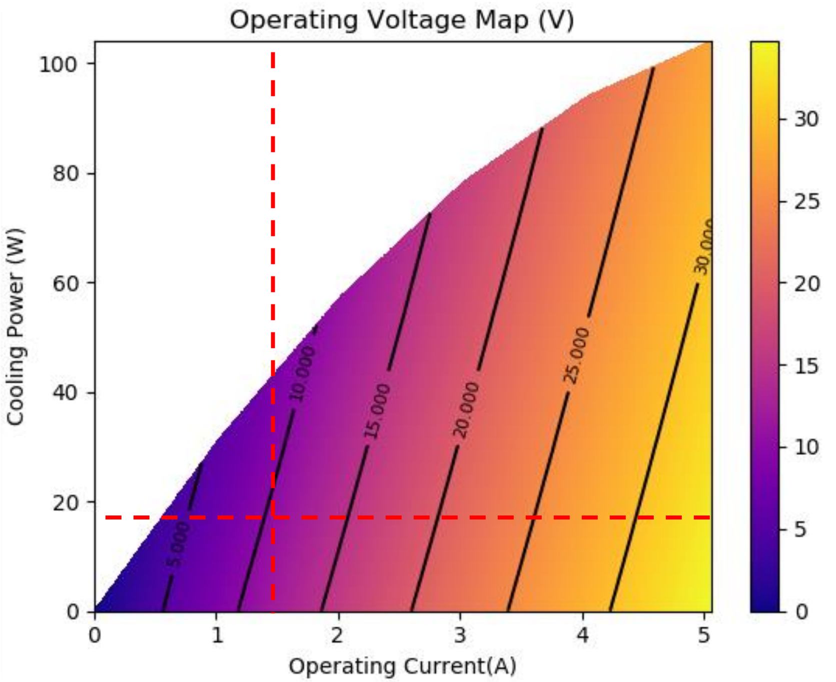

| Part Number | Wakefield Solutions HSF-55-45-B-F |
|---|---|
| Footprint | 55 mm x 55.1 mm |
| Thermal resistance | 0.51 K/W |

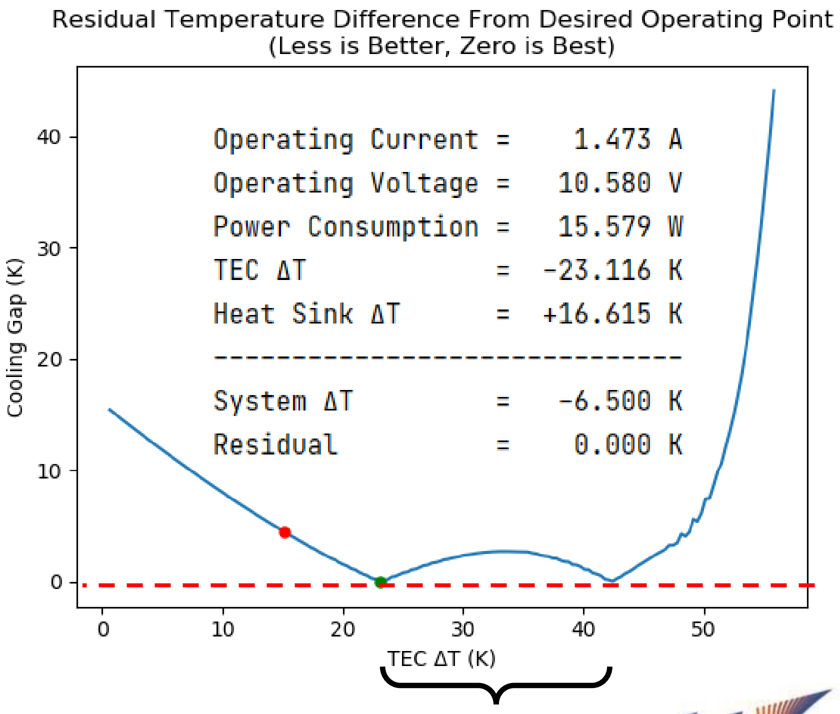
For this small of footprint,
this is the best we could find.

# Peltier Calculation (Real Case)

- This time we use the real heat sink and a double heat sink from RMT Ltd. with "ideal" $Q_{max}$ of 104 W.

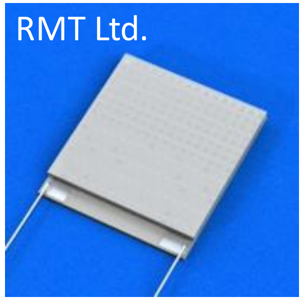



This area is overcooling, so there is some margin

# Thermal Management Performance – TEC




| Type | Parameters | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | ΔTmax [K] | Qmax [W] | Imax [A] | Umax [V] | τ [s] | R [Ohm] | Cold Size [mm$^2$] | Hot Size [mm$^2$] | Height [mm] |
| **2x1MC06-142-03** | **32** | **28.16** | **2.14** | **18.51** | **0.95** | **5.03** | **25.0x25.0** | **25.0x25.0** | **1.39** |

Thot = 300.0 [K], AIR, Heat Sink

| Module 1 Operating Point #1 | |
|---|---|
| Max Heat Load (W) | 17.0 |
| Cold Side Temp (K) | 293.50 |
| **Cold Side Temp (°C)** | **20.35** |
| Heat Sink Temp (°C) | 43.45 |
| TEC ΔT (K) | 23.10 |
| **System ΔT (K)** | **6.50** |
| Current (A) | 1.47 |
| Voltage (V) | 10.6 |
| **Power Consumption (W)** | **15.6** |

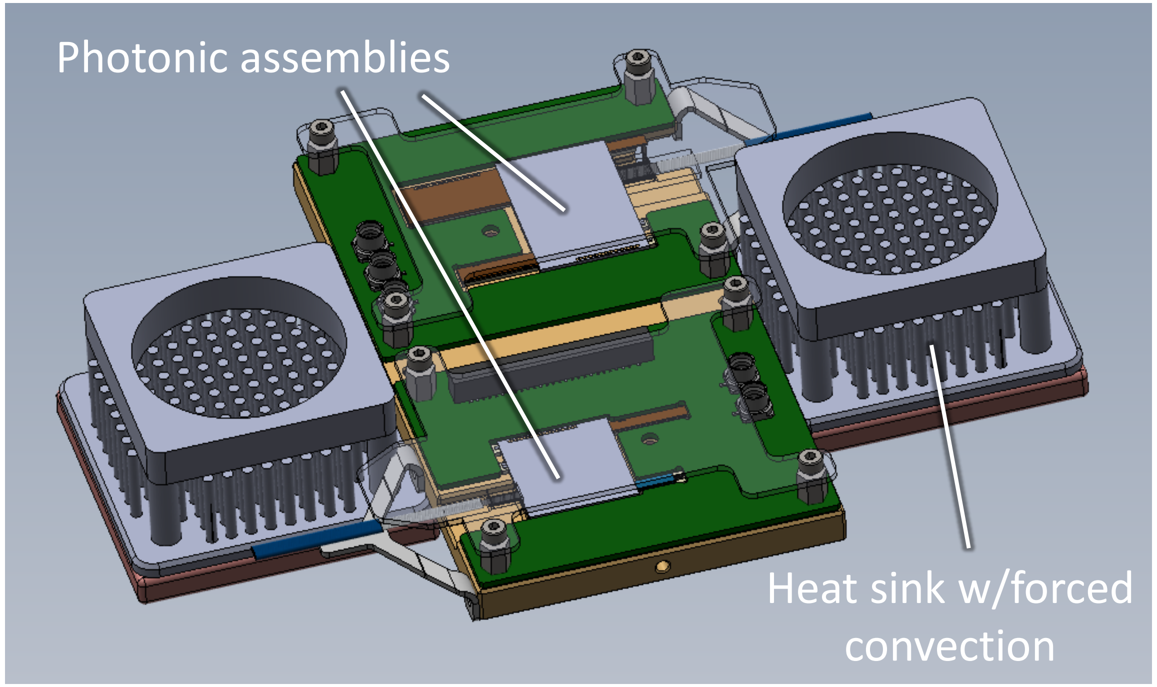
| Module 1 Operating Point #2 | |
|---|---|
| Max Heat Load (W) | 17.0 |
| Cold Side Temp (K) | 298.15 |
| **Cold Side Temp (°C)** | **25.00** |
| Heat Sink Temp (°C) | 39.91 |
| TEC ΔT (K) | 14.91 |
| **System ΔT (K)** | **1.85** |
| Current (A) | 1.11 |
| Voltage (V) | 7.8 |
| **Power Consumption (W)** | **8.6** |

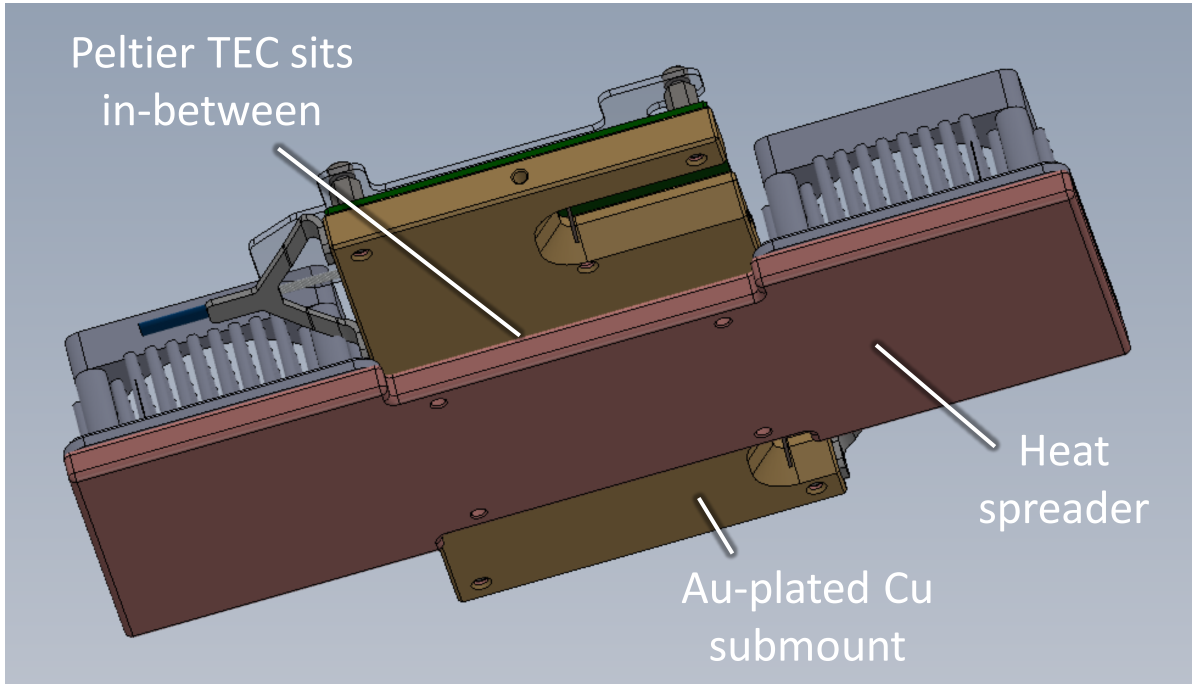
System ΔT is the difference in temperature between the cold side of the TEC and the ambient environment. In this case, ambient was taken as 300 K.

Thermal resistance of **~ 0.51 K/W** to ambient is assumed. The rest of the system will need to guarantee this.

# Thermal Management – Mechanical Design

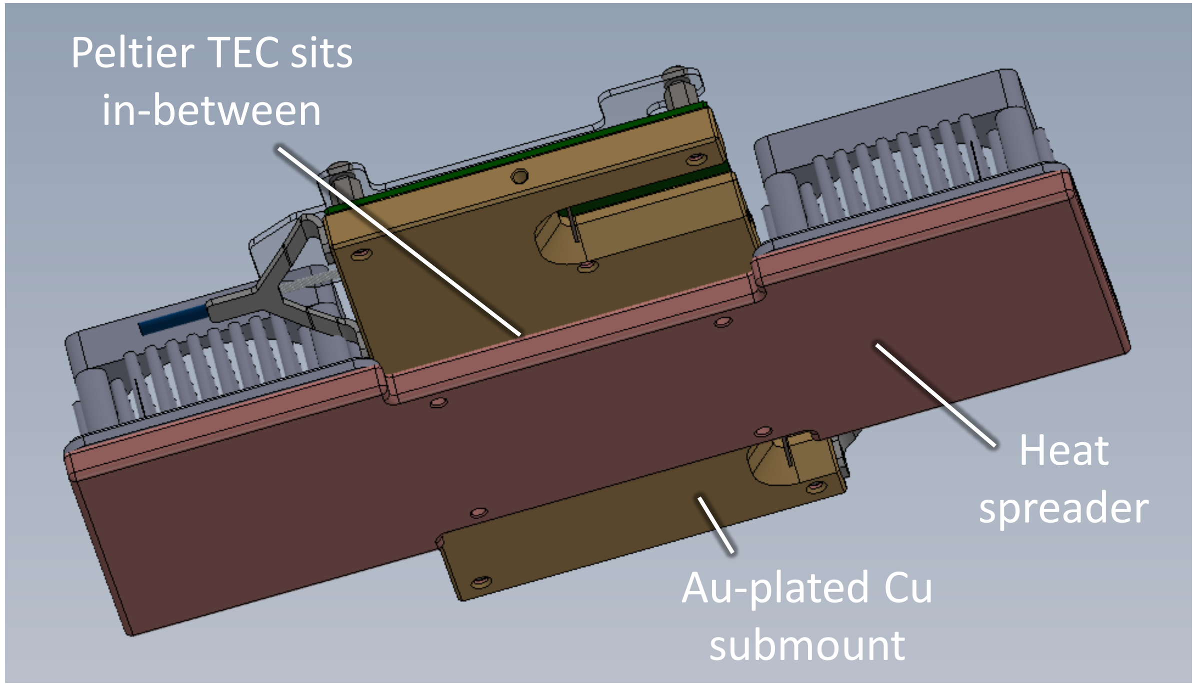
## 5G transceiver to be mounted in drone




The initial design was then adapted to include some elements of heat piping in anticipation of a system-wide heat pipe design for the final drone with collective heat sinking taking advantage of, e.g., drone propellers.

# Thermal Management Sizing – Heat Pipe



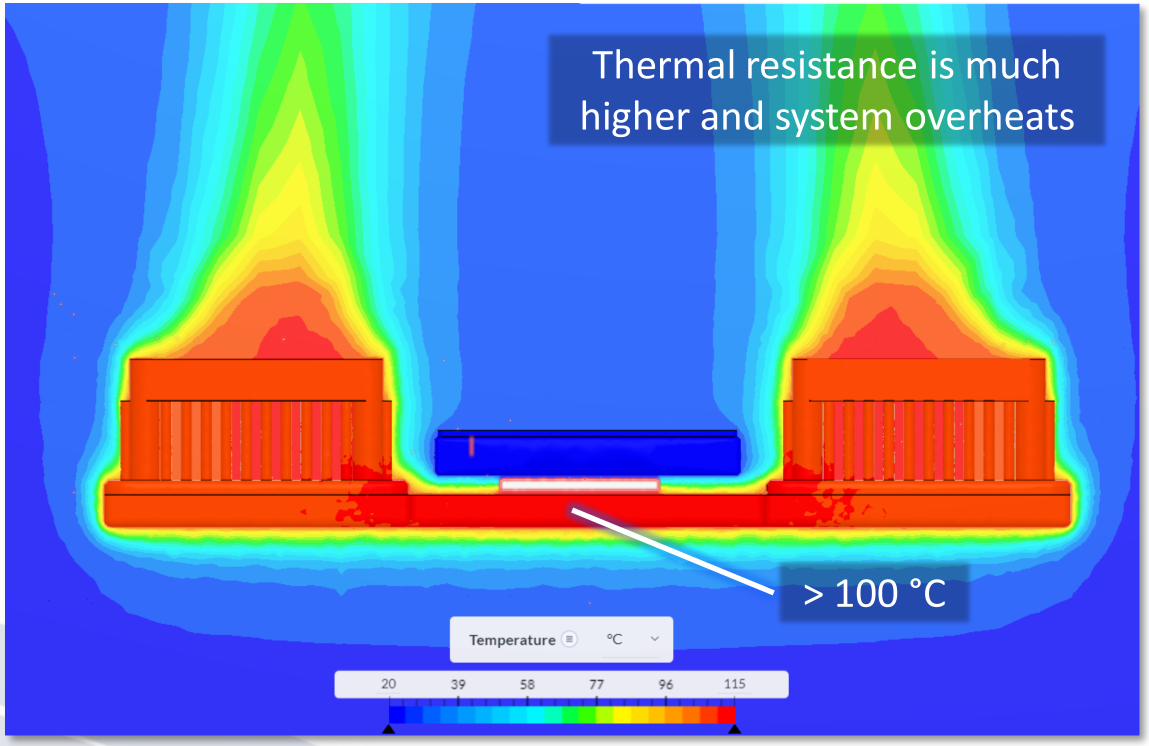

| Module 1 Heat Dissipation | |
|---|---|
| Heat Spreader Width (mm) | 40 |
| Heat Spreader Thickness (mm) | 7 |
| Incremental Thermal Resistance (K/W·mm) | 9.3E-3 |
| Longest Path TEC -> Heat Sink (mm) | 22 |
| Heat Spreader Thermal Resistance (K/W) | 0.20 |
| Heat Sink Thermal Resistance (K/W) | 0.81 |
| Total Thermal Resistance (One Side) | 1.01 |
| **Total Thermal Resistance (Two Sides in Parallel)** | **0.51** |

Original heat sink and fan replaced with lower-profile version:
HSF-55-27-B-F
(Thermal Resistance = 0.81)

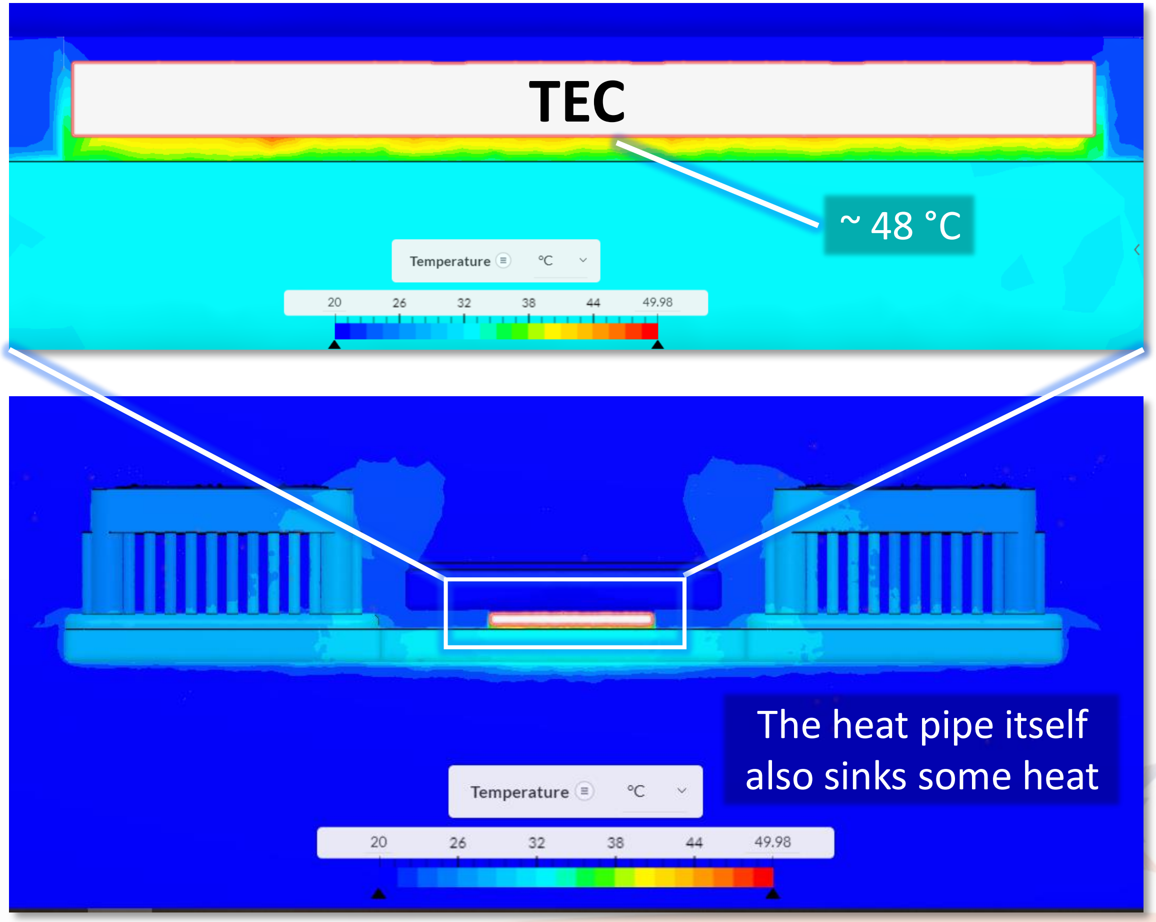
This is based on a worst-case analysis.
In reality, the heat dissipation of the heat spreader itself will help with cooling.

# Thermal Management Verification

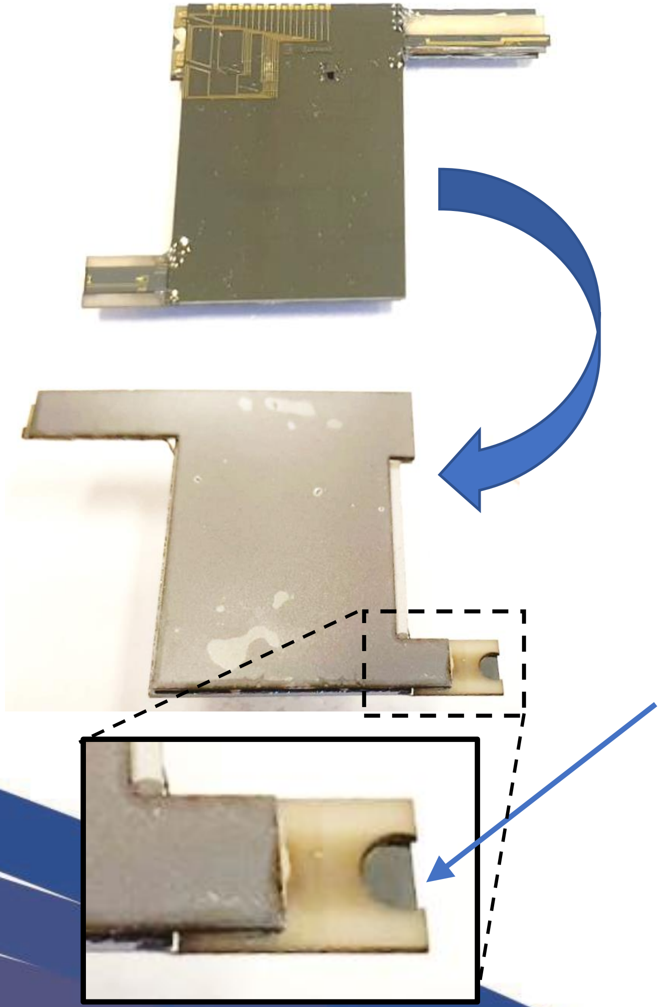
Fans off



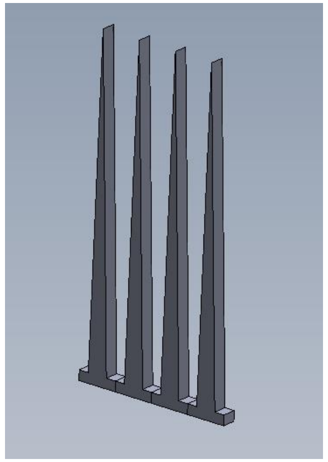

Fans on



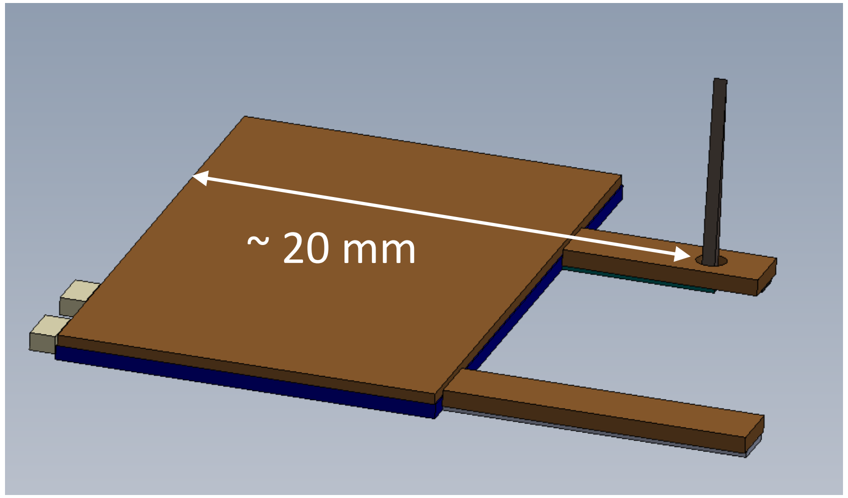
# Antenna Rod Placement –
## High-level Problem Description



Antenna rods



Underside of multi-chip assembly

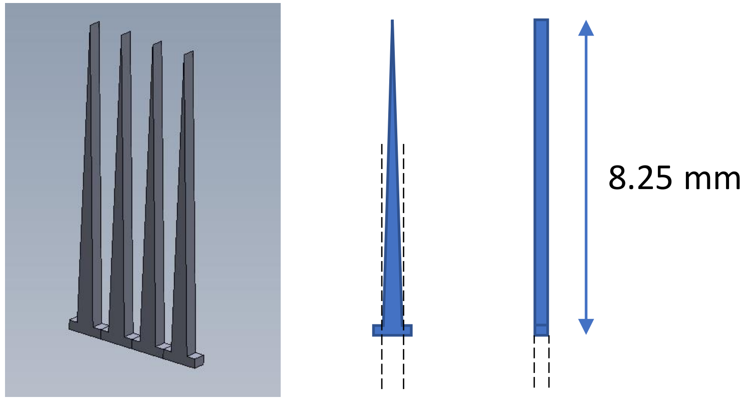



- We need to attach antenna rods to the underside of a multi-chip assembly with accuracy on the order of 100 µm
- Attach is with UV cure adhesive (to be pre-dispensed)
- Initially, we will only do single rods, but eventually we will need to do arrays of 1 x 4 and 4 x 4

# Antenna Rod Placement - Process Flow

Antenna rods

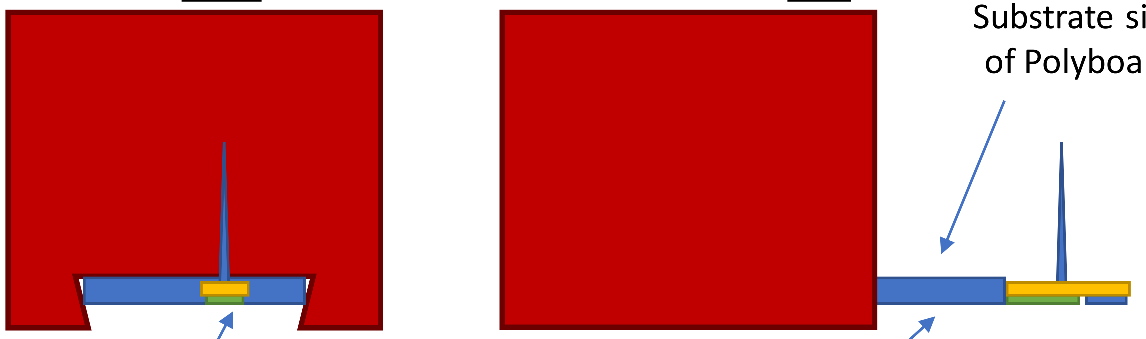
Front Side



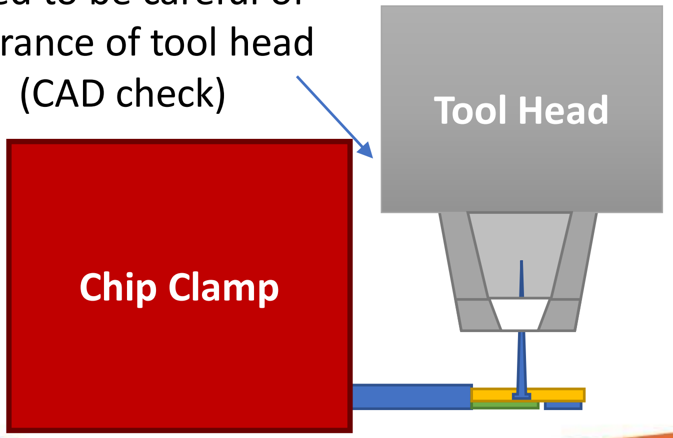

0.7875 $mm^3$ -> 1.835 mg

Assembly Fixturing
(Standard chip clamp flipped over)

Front Side




Need to be careful of clearance of tool head (CAD check)



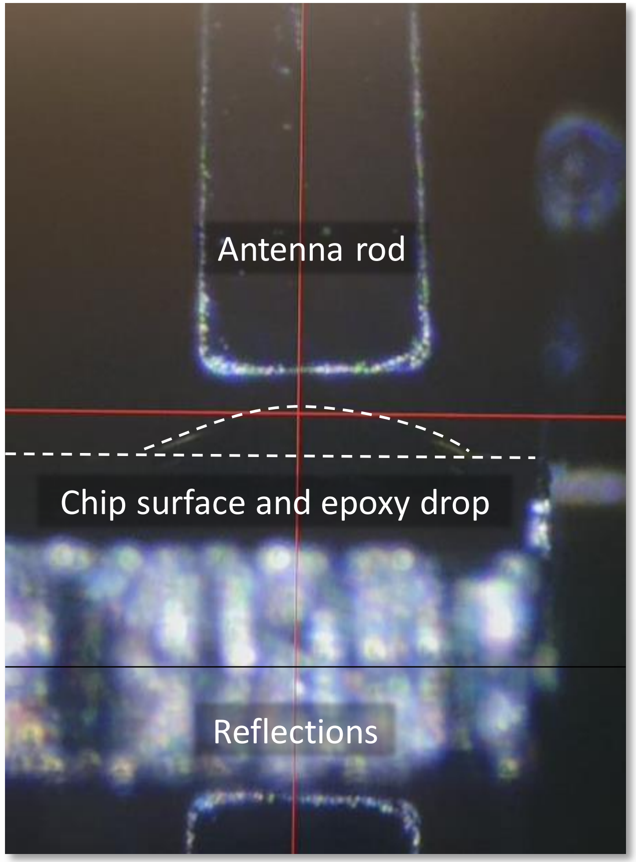

**Process Flow**

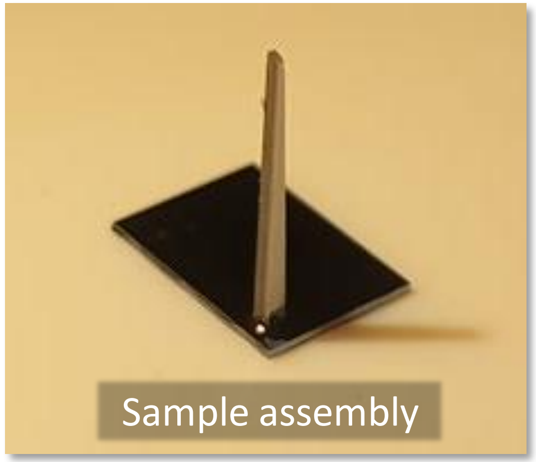
1) **Pick up or manually load antenna rod into vacuum tool**
2) **Align and place**
3) **UV cure**

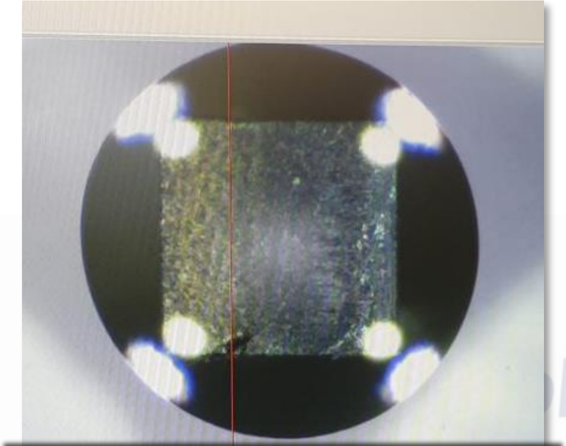
# Antenna Rod Placement – First Trials

### Tool Head Prototype


### Side camera during placement



# Questions???

phix PHOTONIC ASSEMBLY

PHOTONICS21
PHOTONICS PUBLIC PRIVATE PARTNERSHIP

*Funded by the Horizon 2020 Framework Programme of the European Union under the Photonics Public Private Partnership*

# TERAWAY Contacts

For more info, visit TERAWAY website

ict-teraway.eu

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