A Wideband Ultra-Low Current Noise Transimpedance Amplifier for Ultrafast Wideband THz Communication

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***Abstract*— This work reports a wideband transimpedance amplifier MMIC with ultra-low input referred noise current. Being based on transferred substrate InP DHBT process, this work achieves a significant leap forward for ultra-low noise transimpedance amplifier design particularly in HBT based processes, in which, low noise characteristic is fundamentally challenging to achieve. Using a low bias current for amplification, the noise current is kept low. As a result, the amplification is achieved without compromising the noise current performance of the circuit. A 3-dB bandwidth from DC to 10 GHz was achieved with a transimpedance gain of beyond 50 dBΩ with a measured input referred noise current density of 3 $pA/\sqrt{Hz}$. To the authors best knowledge, this is the lowest reported input-referred noise current density for InP DHBT based TIA, covering such wide bandwidth.**

***Keywords*— Transimpedance amplifier (TIA), input referred noise current density.**

I. Introduction

Ultra-low-noise performance is a crucial factor in determining the maximum data rate for a given optical receiver sensitivity. Low-noise TIA performance can improve the receiver module in either or both data rate and T_x/R_x distance. The eventual benefit of such a low noise TIA is the possibility of widening the bandwidth for higher data rate applications. Traditionally, the low noise TIA were implemented in SiGe HBT [1], CMOS [2], InP DHBT [3] with SiGe HBT based TIA reaching up to 5.5 $pA/\sqrt{Hz}$ of input referred noise. This is the state-of-the-art in these technologies for TIA circuits. However, combining a TIA with low noise feature together with high linearity is technologically challenging for the aforementioned technologies. InP HBTs, have shown that highly linear and low noise operation can be possible together in a single chip [4,5,6]. This work reports on the design and fabrication of an ultra-low-noise wideband transimpedance amplifier (TIA) for receiver module.

Due to the large distance between signal emission and reception and considering photodiode sensitivity, a requirement of 100 nA is set for the input noise current of the TIA with an ultimate bandwidth of 20 GHz. Such low current levels are important to increase the sensitivity of the receiver (R_x) modules. This translates to an input referred noise current of $1 pA/\sqrt{Hz}$, which is well below state-of-the-art (SOA), as indicated above.

Such an achievement in InP DHBT based circuit is novel and very appealing, since InP DHBT based circuits have shown immense potential with high RF output power generation along with relatively low noise performance [4,5,6] and high bandwidth. Not only a low noise TIA development would enhance the portfolio of InP DHBT based circuits, but also enable future full MMIC T_x/R_x module development that are either monolithically grown or hetero-integrated MMIC connected via flip chip or bond-wires. The TIA aims at a flip chip integration in PCB as a proof of concept, success of which will eventually lead us to a fully integrated MMIC.

II. Technology

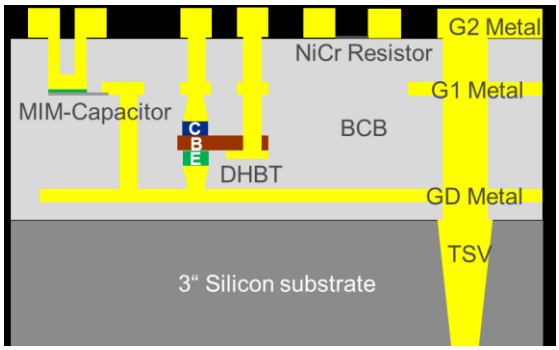

Fig. 1. Simplified layer stack of transferred substrate process

The circuit mentioned in this article is based on the 3-inch FBH transfer-substrate InP-DHBT technology as shown in Fig. 1. In this process, emitter, base and ground layers of the HBT are processed before the complete structure is flipped and bonded on a carrier silicon wafer using the in-house BCB

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bonding process. After substrate removal, collector contacts are processed aligned to the emitter contacts. In the first planarization step, the base, collector and emitter are connected to the first metallization layer G1 through a via and a galvanic step. To realize the passives, SiN based Metal-insulator-metal capacitors (MIMs) and NiCr based thin-film resistors (TFRs). Finally, the whole structure is planarized once more with BCB and the second metallization layer is processed. All lithography steps are performed with by a Niko i-line Stepper. The epitaxy is industry-grade DHBT epitaxial layers on 3-inch semi-insulating InP substrates. The base region is a 30 nm thick InGaAs layer optimized for lower transit time through grading the p-doping from the emitter side to the collector side (high to low). The collector epitaxial thickness is 80 nm which allows for a breakdown voltage of 4V.

III. Circuit Design

Since a low noise generating circuit is dependent on low noise transistors operating at ultra-low bias points, the design of the TIA is chosen to be simplistic with minimum number of transistors that meets the forward transimpedance requirement. An important aspect is to employ transistors with a high gain at very low bias operating points. This defines the choice of transistor devices. Several topologies exist to design an ultra-low noise TIA, namely, distributed architecture, Cherry-Hooper and feedback based. Since feedback-based TIA can be implemented using small number of transistors, the control of the noise generation depends on the bias of the transistor.

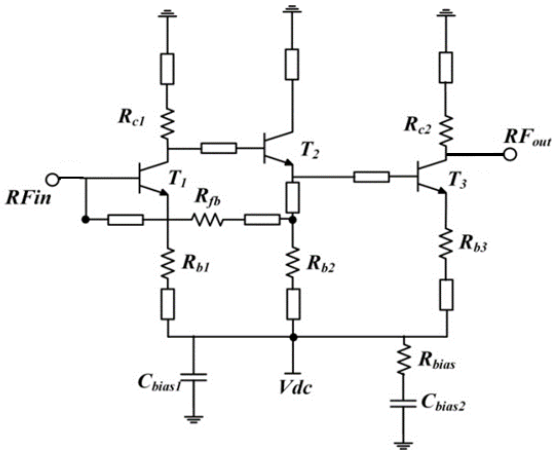

Fig. 2.Simplified circuit schematic

The design used in this work is shown in Fig. 2. The first two transistors form the gain stage of the feedback loop, which acts as the current to voltage converter. The resistive feedback helps to provide a positive feedback loop, thereby increasing the gain performance. The final stage transistor acts as the gain booster with voltage-voltage conversion between its input and output. To reduce the noise generated by the TIA, the bias resistances are chosen such that only 5 mA of collector current flows through the transistor T_1, much lower than its optimum current of 12 mA (I_c for highest f_{max}). The feedback resistor R_{fb} was chosen to be 210 Ω for optimum noise and gain performance. Resistors R_{C1}, R_{b1} and R_{b2} set the bias to the transistors T_1 and T_2. Finally, the bias for transistor T_3 is adjusted by R_{b3} and R_{c2} for optimum gain performance. The circuit is biased with only one DC source.

In order to reduce the noise generations, FBH has developed a new process line, which aims at dramatically reducing the base resistance of the transistors, which are currently more than 40 Ω. According to our estimate, we require a base resistance under 10 Ω in order to be close to an input referred noise current of 1 $pA/\sqrt{Hz}$. The final S-parameter simulations are shown in Fig. 3.

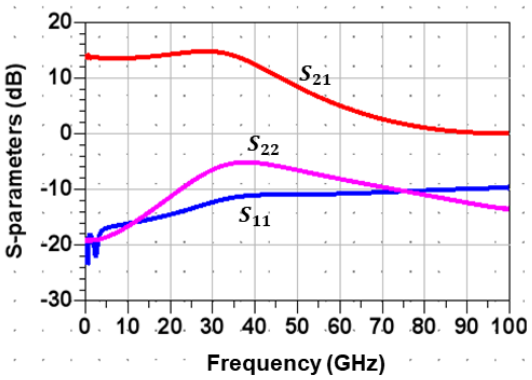

Fig. 3. The circuit simulation for S-parameter of the TIA

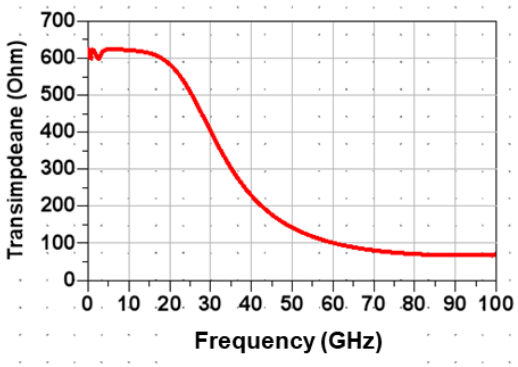

Fig. 4. The circuit simulation for Transimpedance gain (a bias voltage of -1.9 V and 30 mA current was used for simulation)

From Fig. 4 the simulations show that the TIA can offer up to 20 GHz of uniform transimpedance of 600 Ω with low current noise of 3 $pA/\sqrt{Hz}$ with the currently available InP DHBT process at FBH. With the future technology circuit runs, FBH aims to provide even lower noise performance. The achieved transimpedance is equivalent to >50 dBΩ up to 20 GHz, which is sufficient of the receiver operation.

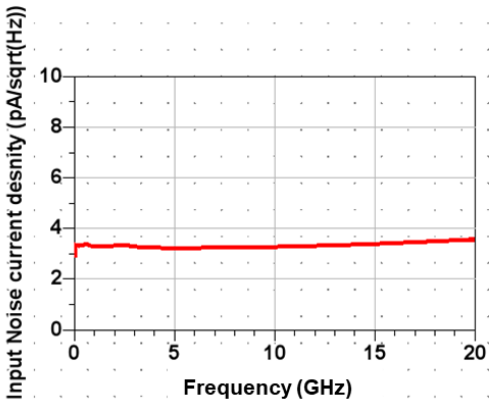

Fig. 5. The circuit simulation for (Input referred noise current (a bias voltage of -1.9 V and 30 mA current was used for simulation)

From Fig. 5, the input referred noise current of the TIA is rather flat across the overall bandwidth of 20 GHz, with a slight increase beyond 10 GHz. This slight increase will be eliminated in a redesign of the TIA, when improved device performance will be available from the FBH InP DHBT process. It is seen from the simulation in Fig. 5 that the input referred noise current requires the new transistors with novel value of base resistance in order to arrive at the envisaged noise performance, which will be done as next steps in the project. The final circuit diagram is given in Fig. 6.

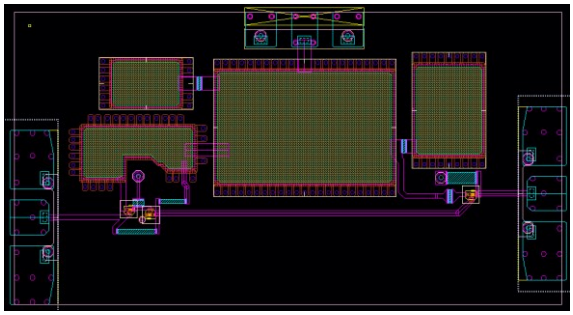

Fig. 6. Picture of the fabricated TIA (extra-large capacitors are added for better DC decoupling) and measures 1.3× 0.7 mm^2

IV. Measurements

The fabricated TIAs small-signal S-parameters have been measured on-wafer and results plotted in Fig. 7. The on-wafer S-parameter measurement has been accomplished using a Keysight PNA-X to 67 GHz with appropriate mTRL calibration down to the probe tips. The measurement provides amplitude and phase results, but only amplitude results are shown in Fig. 7. The forward gain $S_{21}$of the TIA exhibits a transimpedance of >52 dBΩ up to 10 GHz. The reflection parameters are also below 10 dB up to 10 GHz and a return loss around 15 dB up to 5 GHz. The kink visible in the S_{11} and the S_{21} is due to capacitance mismatch from simulated values and will be eliminated in the re-design.

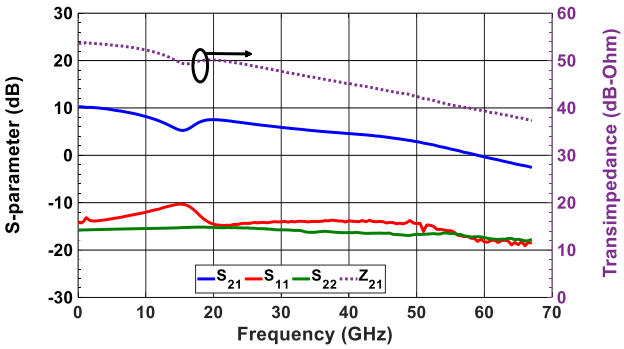

Fig. 7. S-parameter measurement of the TIA (1-Gen)

Based on the noise measurement methodology in [8], we have fully characterized the circuit and its noise performance. An input referred noise spectral density equal to 2.95 and 2.98 $pA/\sqrt{Hz}$ at 4 and 5 GHz, respectively, has been measured and determined for this circuit. Fig. 8 shows the measured result vs simulation, the noise performance is approximately 3 $pA/\sqrt{Hz}$ up to 10 GHz, after which it starts to increase. This is mainly because the transimpedance and forward gain (S_{21}) decreases beyond 10 GHz. In future versions, the transimpedance gain of the TIA is targeted to exhibit flat gain beyond 20 GHz, which will enable a flat response of the input referred noise current in the TIA up to 20 GHz. With improvement in transistor technology the absolute value of the noise is targeted to be of the order of 1 $pA/\sqrt{Hz}$.

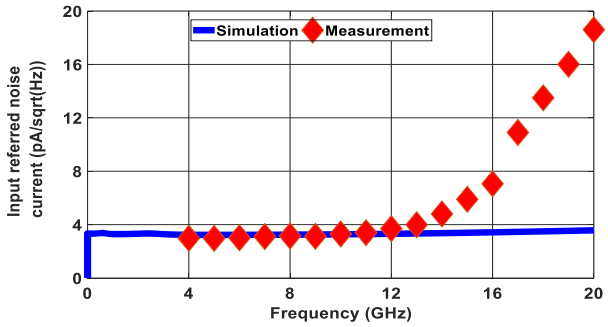

Fig. 8. Input referred noise current measurement vs simulation of the TIA (1-Gen)

V. TIA Assembly for Receiver System

Fig. 9 shows the fully assembled R_x module containing the TIA, as highlighted by the red box. The TIA is connected after a photoconductive antenna (PCA) via bond wire and the output is fed into a coplanar line for reception. The basic idea is to convert the low magnitude current reception from the PCA and convert it to a voltage signal to the coplanar line. The TIA along with neighboring circuitry in the red box is presented clearly in Fig. 10. The assembly has been performed at PHIX in The Netherlands.

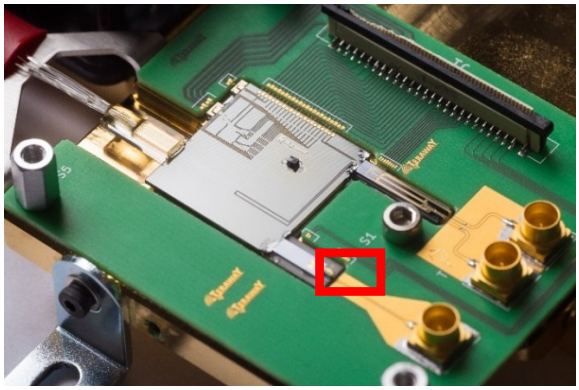

Fig. 9. Full receiver assembly with TIA highlighted (red box)

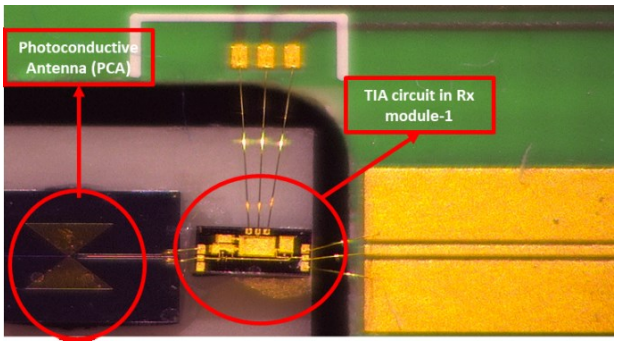

Fig. 10. TIA connected to the assembly PCB zoomed into the red box of Fig. 9

VI. Conclusion

In this work, a wideband transimpedance amplifier has been designed, fabricated and measured for the project Teraway which exhibits ultra-low input referred current noise performance of 3 $pA/\sqrt{Hz}$ with a wide bandwidth of beyond 10 GHz and transimpedance gain of more than 50 dBΩ. Apart from exhibiting the state-of-the-art lowest level of input referred noise current, the circuit achieved significant bandwidth. These results successfully satisfy the first trial specifications of the EU Teraway project.

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